Open NAND Flash Interface Specification: NAND Connector

Connector Revision 1.0
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This 1.0 revision of the Open NAND Flash Interface NAND Connector specification ("Final Specification") is available for download at www.onfi.org.

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For more information about ONFI, refer to the ONFI Workgroup website at www.onfi.org.

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1. Introduction

1.1. Purpose and Scope

This specification defines the standard NAND flash module form factors, and the form, fit and function of the standard NAND module connectors for the NAND flash modules. It contains the connector pin assignments, mechanical, electrical and environmental requirements. The intention of this document is to enable connector, system, and flash module designers and manufacturers to build, qualify and use the NAND module connectors as the standard interfaces to plug the NAND flash modules into PC's and other systems.

1.2. Connector Overview

Driven by different form factor and cost requirements, two different connectors and module form factors are defined in this specification to enable the applications of NAND module in desktop and mobile platforms, as well as other systems.

A 78-pin, 1.0 mm pitch vertical through-hole connector, similar to the existing DDR2 connector, is defined for applications where a module vertically enters the connector, perpendicular to the system board such as in a desktop computer.

A 78- pin, 0.6 mm pitch right-angle surface-mount connector, similar to the existing SO-DDR2 connector, is defined for applications that require a right-angle entry of the module into the connector, parallel to the system board such as in a mobile computer.

1.3. References

The following references provide normative requirements as specified in the body of this specification:

- Open NAND Flash Interface Specification Rev 1.0. www.onfi.org
- Open NAND Flash Interface Specification Rev 2.0. www.onfi.org
- EIA-364-1000.01: Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets used in Business Office Applications. www.eia.org

1.4. Terms and Definitions

Term	Description
EIA	Electronics Industry Alliance
DDR2 connector	240-pin, 1.0 mm pitch vertical connector; refer to customer drawings from connector manufacturers
ONFI	Open NAND Flash Interface
DUT	Device under test
NAND module	Module on which NAND memory packages are placed, used with the NAND module connector
NAND module connectors	Connectors defined in this specification, including both the vertical and right-angle connectors
Right-angle connector	A connector that accepts a module parallel to the system board
SO-DDR2 connector	Small-outline DDR2 connector with a right-angle entry of the module into the connector; refer to customer drawings from connector manufacturers
System board	PCB on which the NAND module connector is mounted
Vertical connector	A connector that accepts a module perpendicular to the system board

2. Signal Description and Pin Assignment

This section describes the signals included in the NAND module connectors, as well as the pin assignments in the connectors and modules.

2.1. Signal Description

Table 1 lists the signals included in the NAND module connector interface. Note that the signals list for the vertical and right-angle connectors is identical.

Signal Group	Signal Name	Count	Description
Data	DQ[15:0]	16	Data bus
Strobes	DQS/DQS# [1:0]	4	Data bus strobe, differential
Clock	CK/CK#[1:0]	4	Clock, differential, see NOTE 1
Control signals	ALE[1:0]	2	Address enable
	CLE[1:0]	2	Command enable
	R/B#	1	Ready/busy
	WP#	1	Write protect
	W/R#[1:0]	2	Write ready, see NOTE 2
	WE#[1:0]	2	Write enable, see NOTE 1
	RE#[1:0]	2	Read enable, see NOTE 2
Chip Enable	CE[7:0]	8	Chip enable
Power and Ground	VSS	24	Ground
	VCCQ	3	I/O power
	VCC	6	Core power
	VREF	1	Reference voltage
Reserved	RFU	4	Reserved for future use
Total Pin Count		78	

NOTE:
1. CK_0 and CK_1 share the same pins as WE_0# and WE_1#, respectively. See Table 2 for pin assignment.
2. W/R#[1:0] share the same pins as RE#[1:0]. See Table 2 for pin assignment.

Table 1 Vertical and Right-angle NAND Connectors and Modules Signal Descriptions

2.2. Pin Assignments

The vertical and right-angle NAND module connectors have the identical pin assignment, as shown in Table 2. Refer to Section 3 for the physical locations of the pins in the connectors and modules. Table 3 defines how the NAND signals are mapped to the DQ bus.

Pin	Signal	Signal	Pin
1	VCC	VCC	40
2	VCC	VCC	41
3	VCC	VCC	42
4	CE_4#	CE_6#	43
5	GND	GND	44
6	DQ0	DQ2	45
7	DQ1	DQ3	46
8	GND	GND	47
9	DQS_0#	CK_0#	48
10	DQS_0	CK_0 / WE_0#	49
11	GND	GND	50
12	DQ4	DQ6	51
13	DQ5	DQ7	52
14	GND	GND	53
15	RFU	R/B#	54
16	RFU	WP#	55
17	GND	GND	56
18	CLE_0	CLE_1	57
19	ALE_0	ALE_1	58
20	GND	GND	59
21	W/R_0# /RE_0#	W/R_1# /RE_1#	60
22	CE_1#	CE_3#	61
23	GND	GND	62
24	CE_0#	RFU	63
25	CE_2#	RFU	64
26	GND	GND	65
KEY			
27	GND	GND	66
28	DQ8	DQ10	67
29	DQ9	DQ11	68
30	GND	GND	69
31	DQS_1#	CK_1#	70
32	DQS_1	CK_1 / WE_1#	71
33	GND	GND	72
34	DQ12	DQ14	73
35	DQ13	DQ15	74
36	GND	GND	75
37	CE_5#	CE_7#	76
38	VCCQ	VREF	77
39	VCCQ	VCCQ	78

Table 2 **Vertical and Right-angle NAND Connectors and Modules Pin Assignment**

CE_0#	DQ[7:0]		CE_2#	DQ[15:8]
CE_1#	DQ[7:0]		CE_3#	DQ[15:8]
CE_4#	DQ[7:0]		CE_6#	DQ[15:8]
CE_5#	DQ[7:0]		CE_7#	DQ[15:8]
ALE_0	DQ[7:0]		ALE_1	DQ[15:8]
CLE_0	DQ[7:0]		CLE_1	DQ[15:8]
W/R_0#	DQ[7:0]		W/R_1#	DQ[15:8]
CK_0	DQ[7:0]		CK_1	DQ[15:8]
DQS_0	DQ[7:0]		DQS_1	DQ[15:8]

Table 3 NAND Signals Mapping to DQ Bus

3. Mechanical Interfaces

This section defines the NAND connector and module mechanical interfaces to ensure form, fit and function.

3.1. Vertical NAND Module Connector

The vertical NAND module connector is defined mainly for applications that require a vertical entry of a module into the connector such as in a desktop computer. Figure 1 shows a 3-dimensional illustration of such a connector.

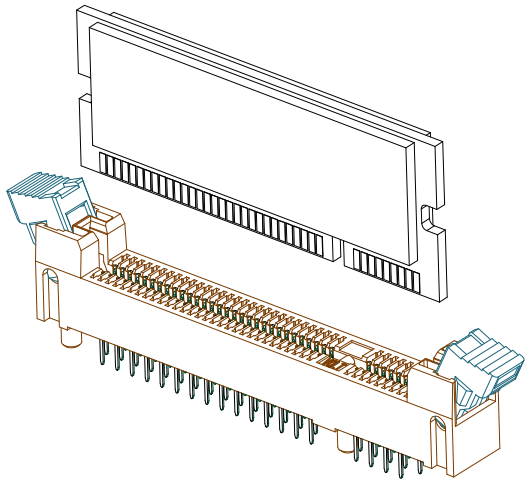


Figure 1 Vertical NAND module connector illustration

This connector is similar to the DDR2 connector, but with 78 pins; connector manufacturers may utilize the DDR2 connector contacts for this connector. The latch design, however, is slightly different from that of the DDR2 connector. The latch for the vertical NAND module connector is smaller, requiring less space.

Figures 2, 3, and 4 show the connector outline dimensions for connectors having locating plastic pegs for the three voltage keying options: 3.3V, 1.8V and X.XV (reserved for future).

The use of metal board locks is also allowed. Figures 5, 6 and 7 provide the connector outlines for connectors with the metal board locks for each of the supported voltages.

Figure 8 illustrates the connector with the latches at the fully open position. The latches must be completely within the shaded areas when fully opened and the system board designer shall make sure no mechanical interference between components on the system board and the latches.

The recommended connector footprints for each of the supported voltages are shown in Figures 9, 10 and 11. Note that these footprints are applicable for both the plastic peg and the metal board lock versions of the connector.

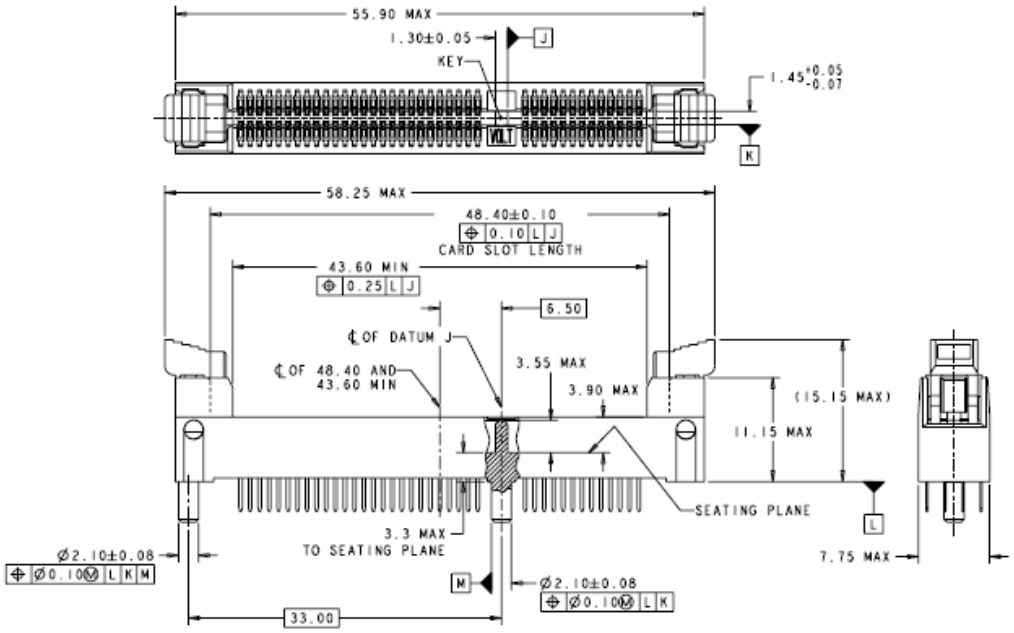


Figure 2 **3.3V vertical NAND module connector dimensions with plastic pegs, shown with latch closed**

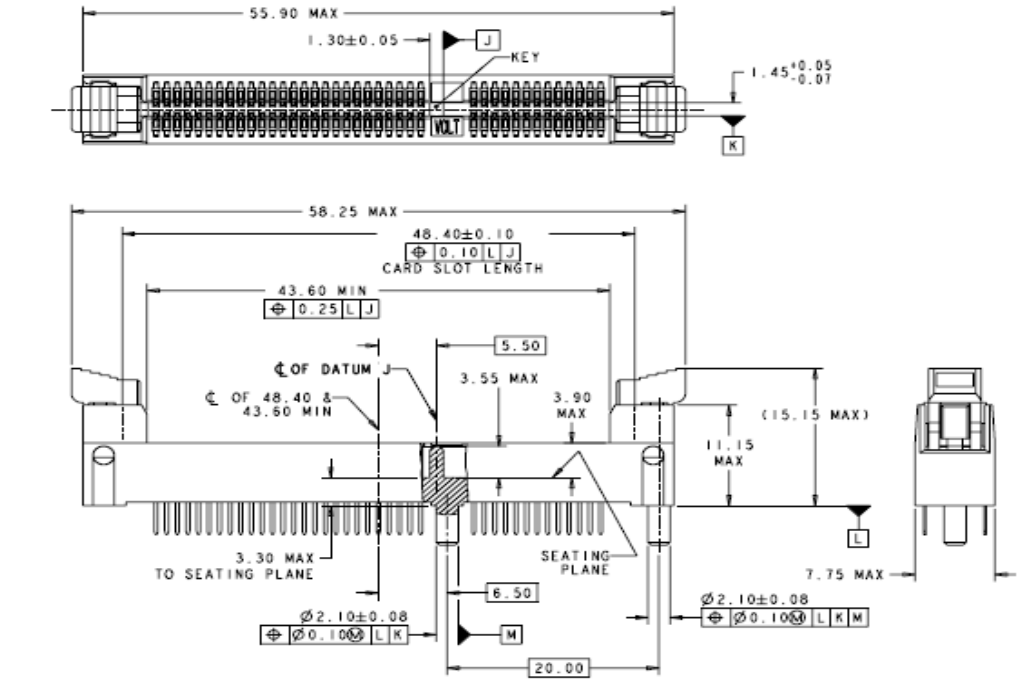


Figure 3 **1.8V vertical NAND module connector dimensions with plastic pegs, shown with latch closed**

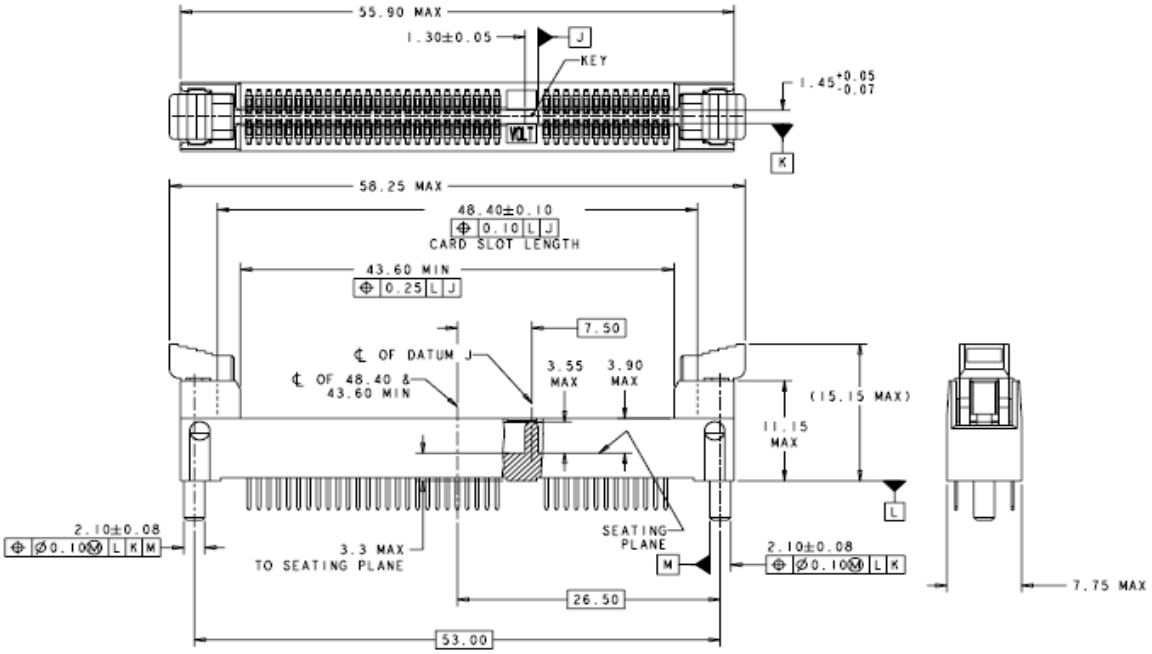


Figure 4 **X.X V vertical NAND module connector dimensions with plastic pegs, shown with latch closed**

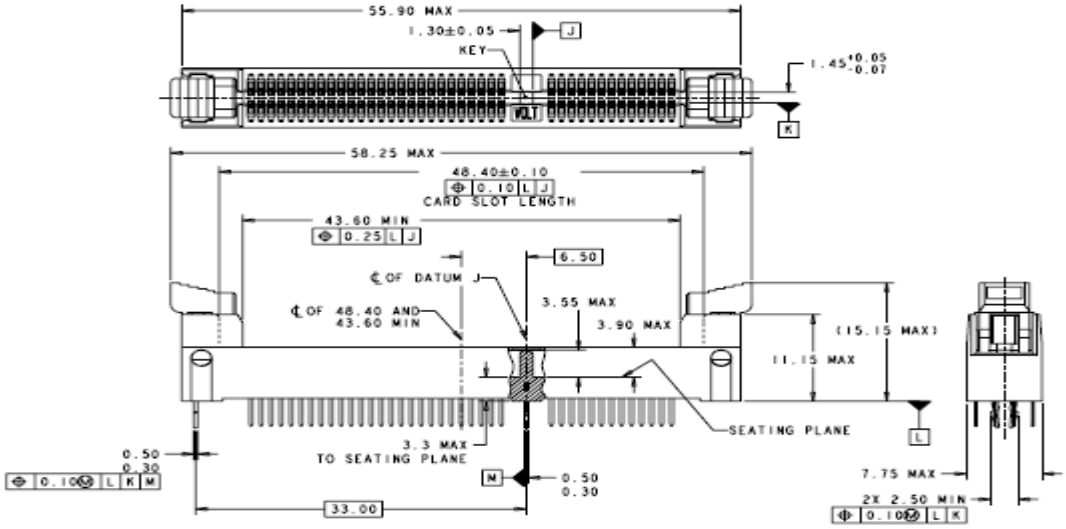


Figure 5 **3.3V vertical NAND module connector dimensions with metal board locks, shown with latch close**

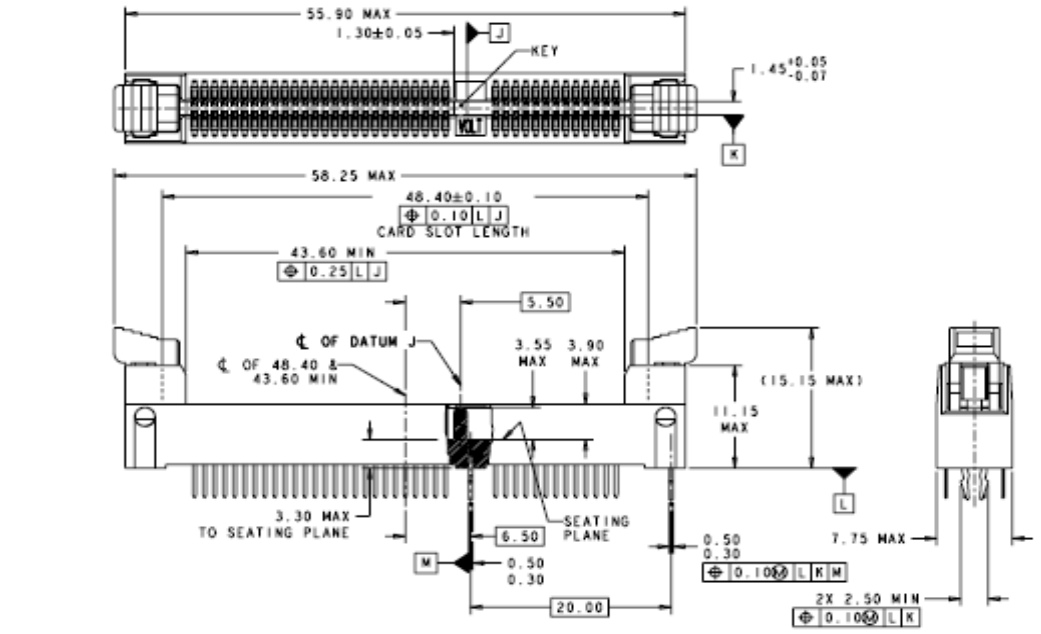


Figure 6 **1.8V vertical NAND module connector dimensions with metal board locks, shown with latch close**

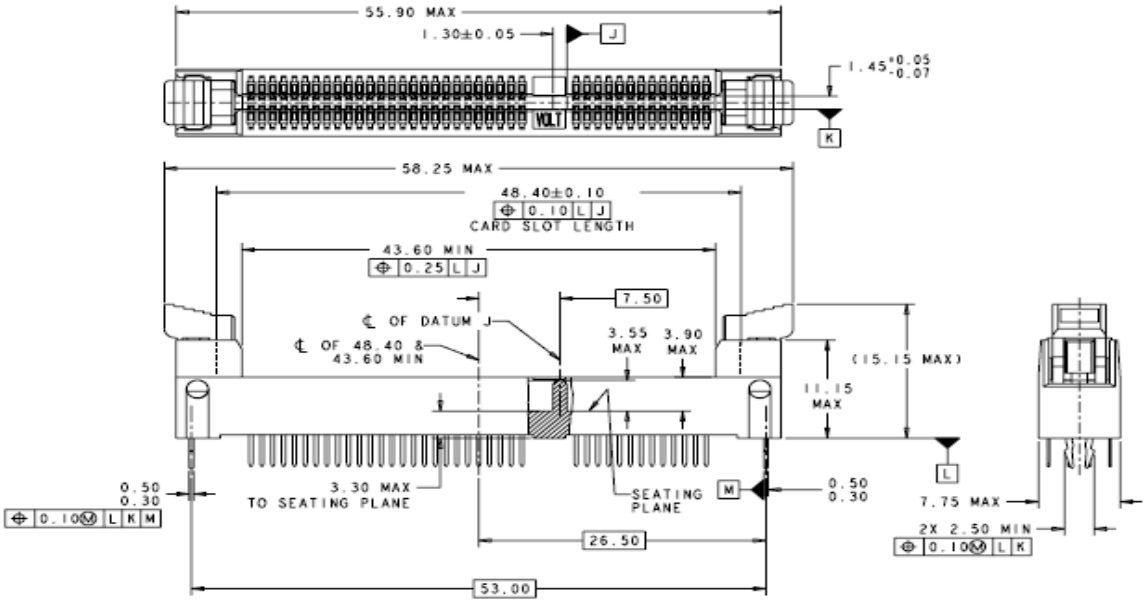


Figure 7 **X.XV vertical NAND module connector dimensions with metal board locks, shown with latch close**

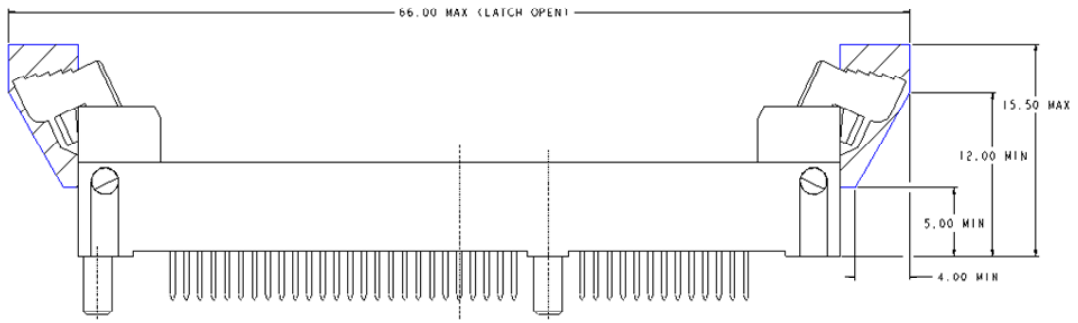


Figure 8 **Vertical NAND module connector with latches open, applicable to plastic pegs or metal board locks versions**

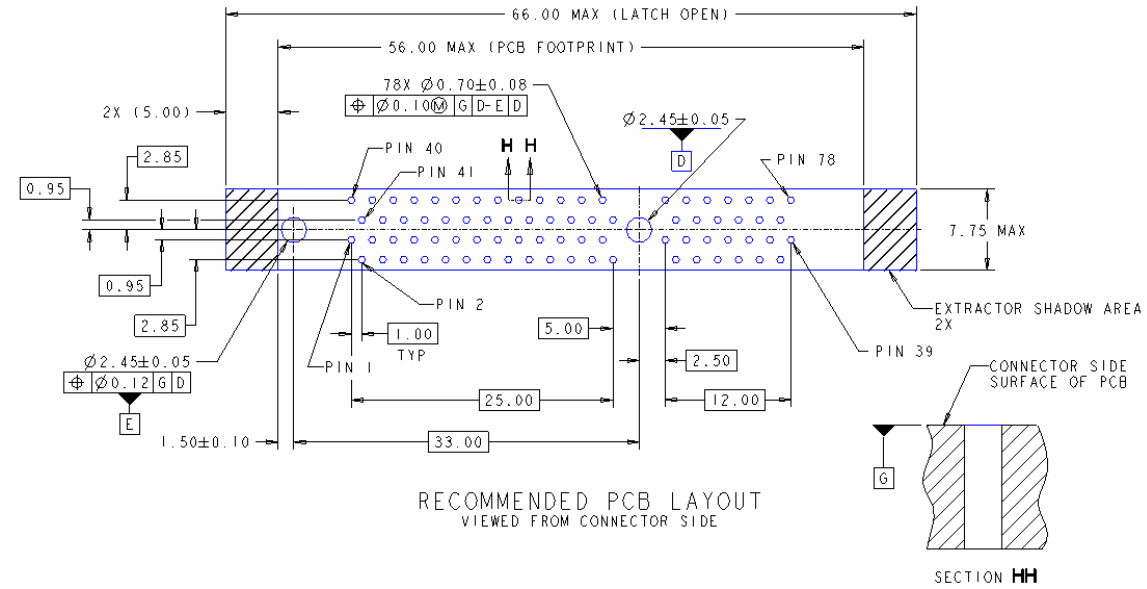


Figure 9 **3.3V vertical NAND module connector footprint, applicable to plastic pegs or metal board locks**

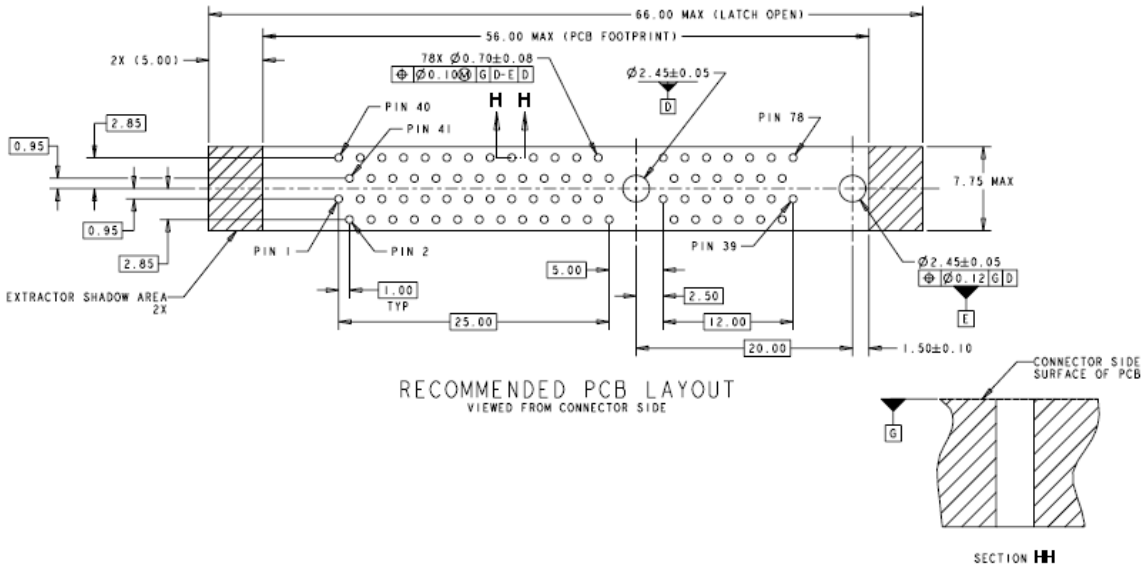


Figure 10 1.8V vertical NAND module connector footprint, applicable to plastic pegs or metal board locks

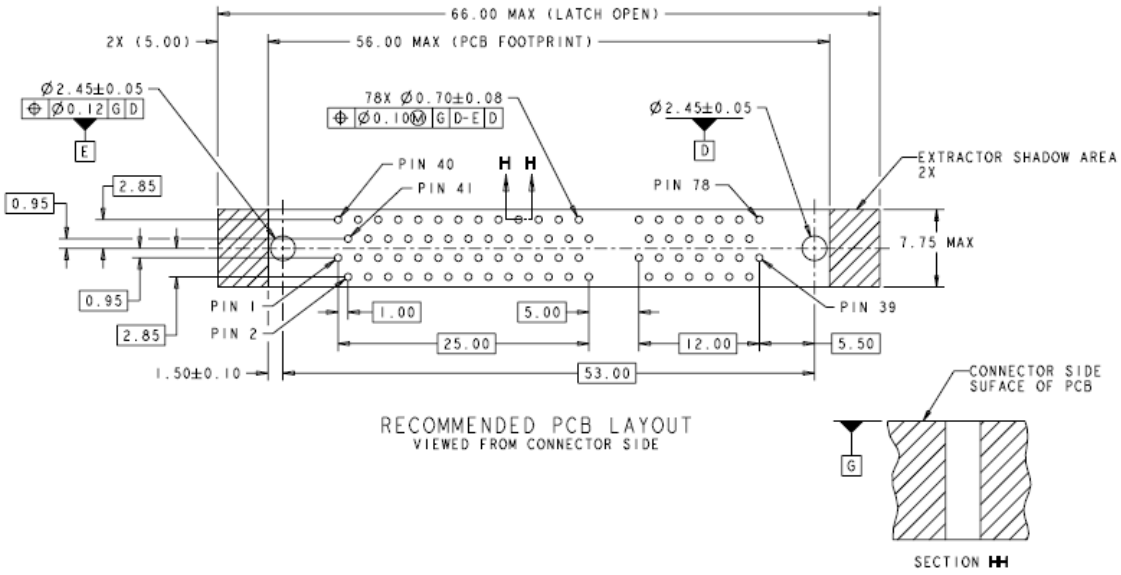


Figure 11 X.XV vertical NAND module connector footprint, applicable to plastic pegs or metal board locks

The vertical NAND module mechanical dimensions are shown in Figure 12. There are three key locations on the module and connector to distinguish three VCCQ voltages: 3.3V, 1.8V, and a future voltage, designated as X.XV. The module key locations are given in Figure 13.

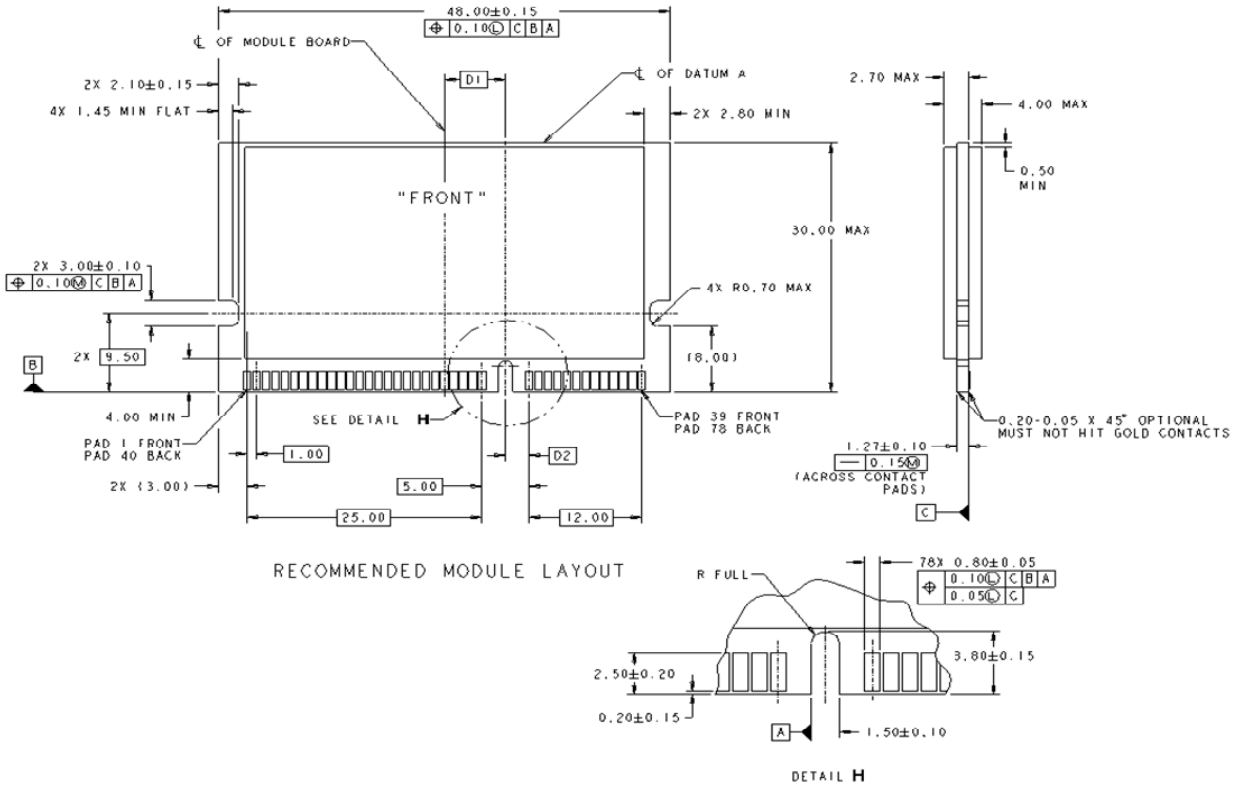
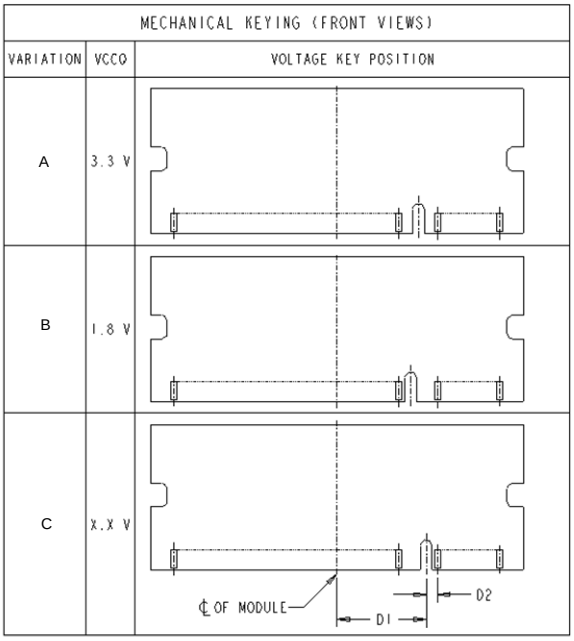


Figure 12 Vertical NAND module dimensions



	A	B	C
D1	6.50 BASIC	5.50 BASIC	7.50 BASIC
D2	2.50 BASIC	3.50 BASIC	1.50 BASIC

Figure 13 Vertical NAND module voltage key positions

3.2. Right-Angle NAND Module Connector

The right-angle NAND module connector, defined mainly for mobile or other small form factor applications, is illustrated in Figure 14. It is similar to the existing SO-DDR2 connector, but with fewer pins (78).

Figure 15 defines the connector outline dimensions. Note that in Figure 15, dimensions AA and BB are allowed to vary based on OEMs' specific needs; the allowable variations are shown in the Variation Table. Figure 16 shows the recommended connector footprint.

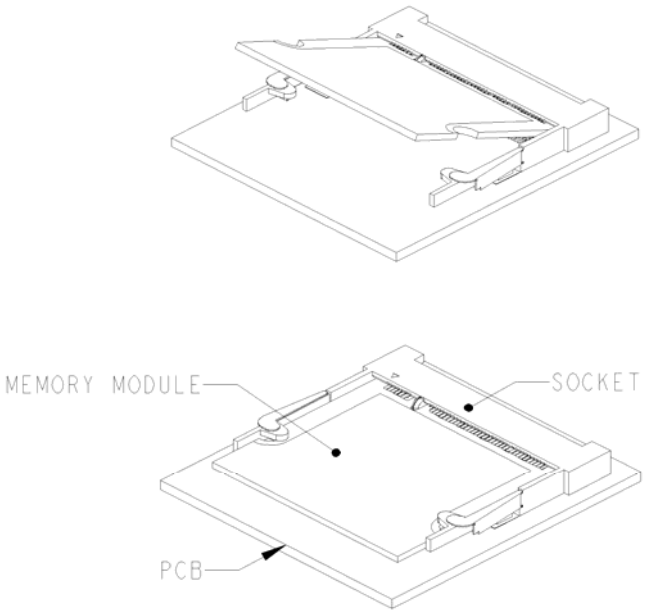
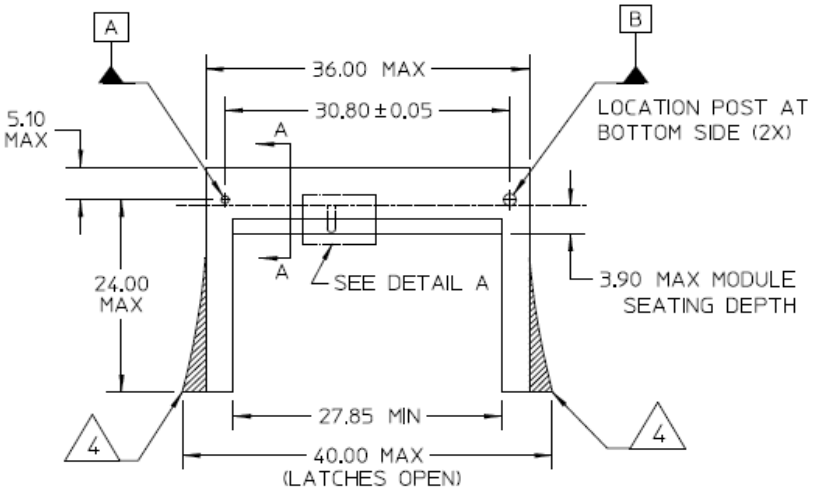
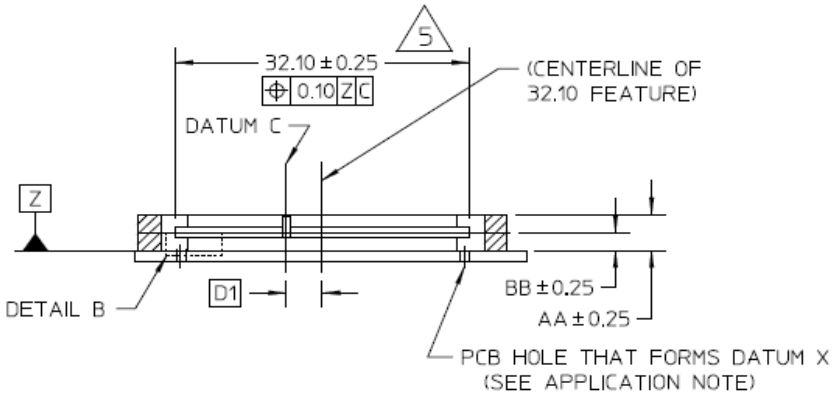


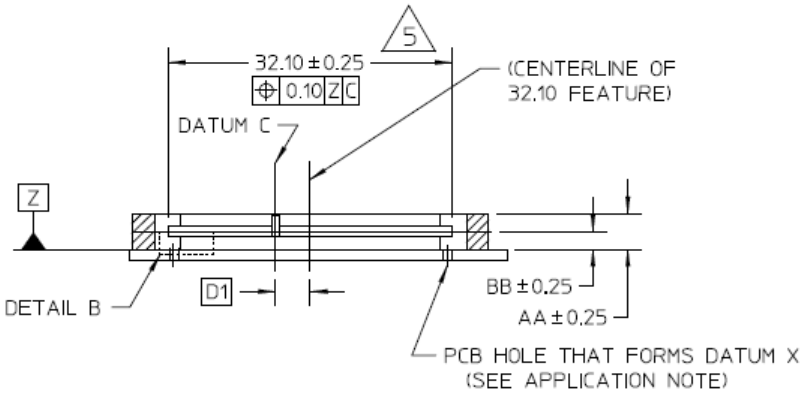
Figure 14 Illustration of Right-angle NAND module connector



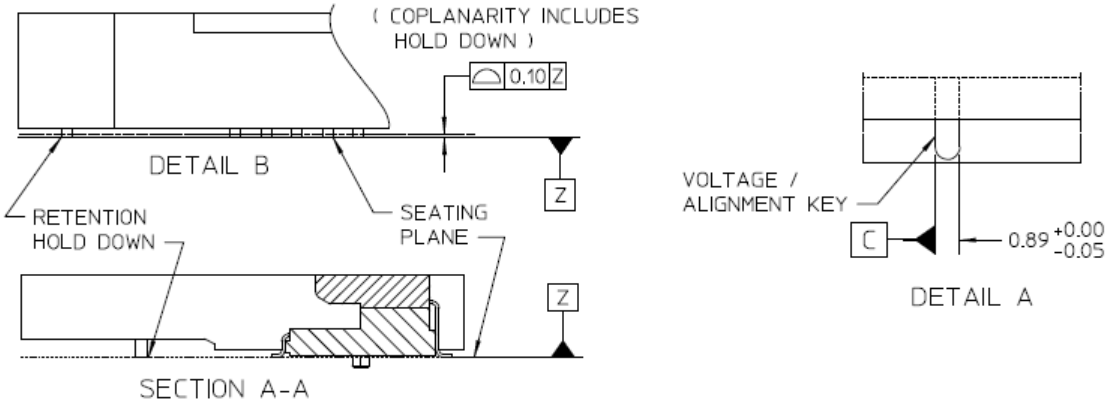
SOCKET TOP VIEW



SOCKET FRONT VIEW



SOCKET FRONT VIEW



RIGHT ANGLE NAND MODULE CONNECTOR INTERFACE DIMENSIONS

	HEIGHT VARIATIONS			
DIMENSION	A	B	C	D
AA	5.20	6.50	8.00	9.20
BB	3.30	4.60	6.10	7.30

	VOLTAGE KEY		
DIMENSION	xA (3.3V)	xB (1.8V)	xC (x.xV)
D1	3.90	2.90	4.90

NOTES :

1. DIMENSIONING AND TOLERANCING CONFORM TO Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS (mm).
3. DIMENSION BB REPRESENTS THE DISTANCE BETWEEN THE CENTERLINE OF THE MODULE AND CONNECTOR CARD SLOT AND THE HOST BOARD SURFACE.

△4 KEEPOUT AREA RESERVED FOR SOCKET EJECTORS - BOTH ENDS

△5 SLOT LENGTH IS SPECIFIC TO THE MATING REGION OF THE SOCKET / INTERFACE THAT FACILITATES ROUGH ALIGNMENT OF THE MODULE.

6. THE FIGURE BELOW IS INCLUDED FOR REFERENCE AND DEPICTS A BOUNDARY AREA (LOCUS) OF A RECTANGULAR GEOMETRY REPRESENTING THE LEAD/CONTACT OF THE CONNECTOR. THIS LOCUS INCLUDES ALLOWANCES FOR POSITION AND SIZE TOLERANCES.

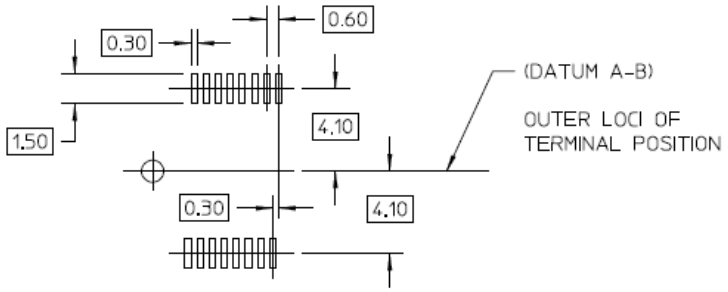


Figure 15 Right-angle NAND module connector Interface dimensions

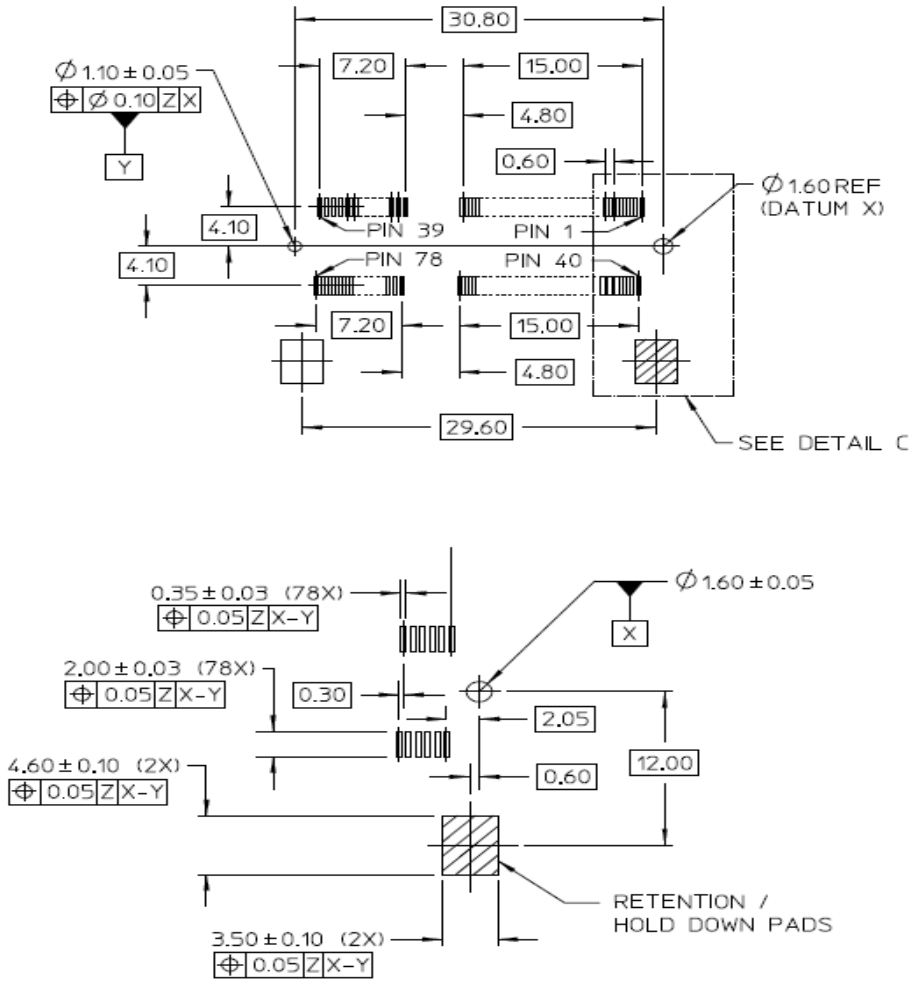


Figure 16 Recommended right-angle NAND module connector footprint

Figure 17 shows the module mechanical dimensions. Note that the module height is denoted as dimension A; three module height variations are defined: 21.5, 32.5, and 36.5 mm. The minimum module height of 21.5 mm is specified to make sure the cut-out features on the module exist for module retention. Figure 18 illustrates the module with a minimum height of 21.5 mm; note that the quarter-circle feature on the module top is present for module retention.

The module height variations together with the voltage key location variations are defined in Figure 19.

To avoid potential shorting between the module traces and metal connector latches, a non-metallization zone is defined on the module, as shown in Figure 20

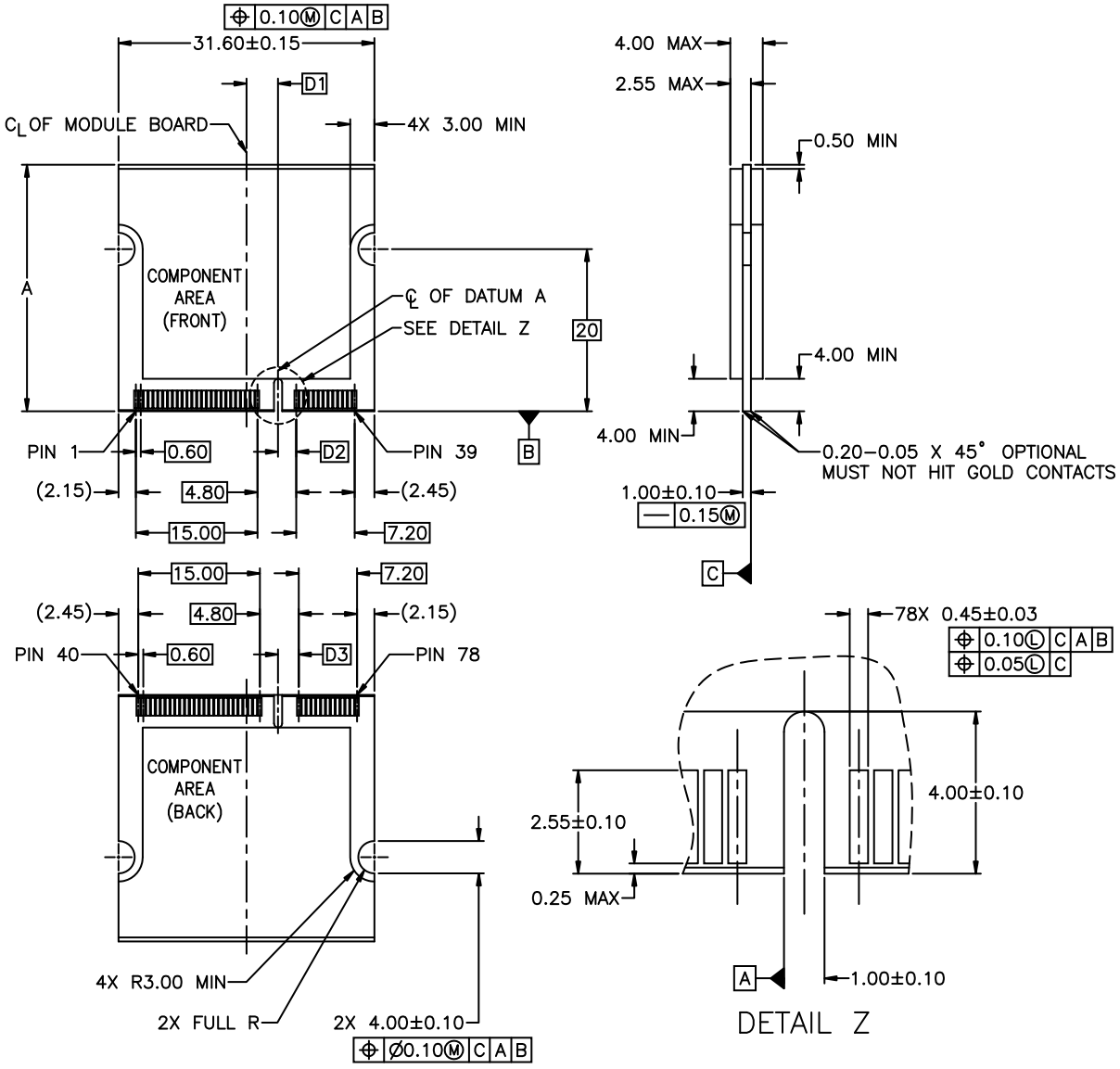


Figure 17 Right-angle NAND module dimensions, variations AA, AB, AC and BA, BB, BC

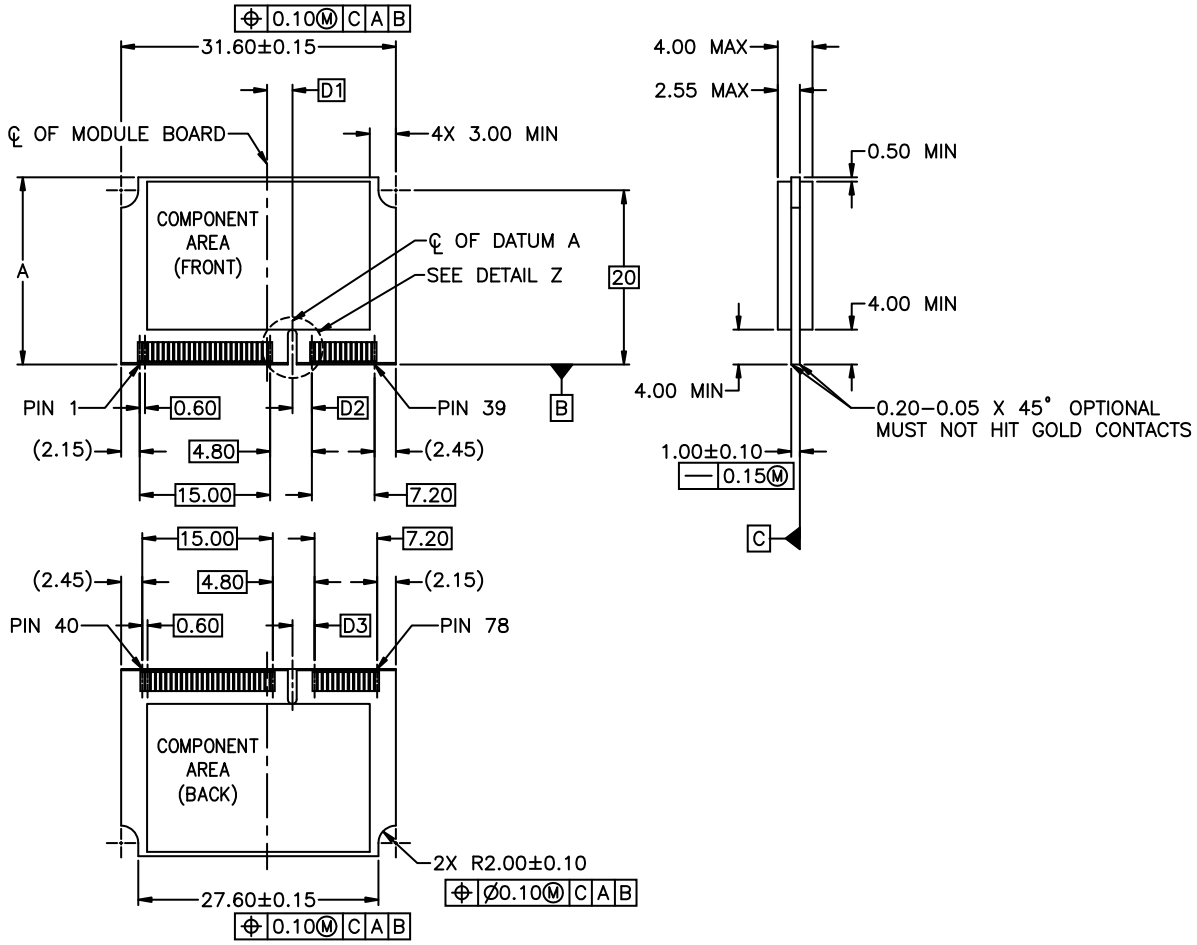
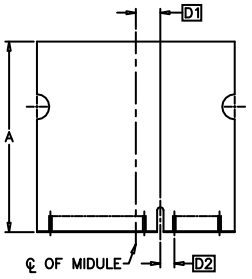
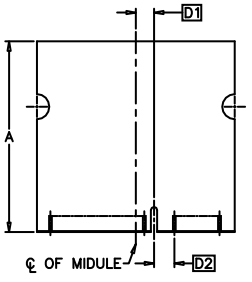
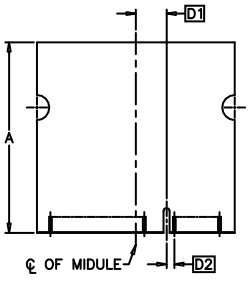


Figure 18 Right-angle NAND module dimensions, variations CA, CB and CC

MECHANICAL KEYING (FRONT VIEWS)		
VARIATION	VCCQ	CENTER KEY POSITION
AA	3.3 V	
AB	1.8 V	
AC	X.X V	

	AA			AB			AC		
A	MAX	NOM	MIN	MAX	NOM	MIN	MAX	NOM	MIN
	36.65	36.50	36.35	36.65	36.50	36.35	36.65	36.50	36.35
D1	3.90 BASIC			2.90 BASIC			4.90 BASIC		
D2	2.25 BASIC			3.25 BASIC			1.25 BASIC		
D3	2.55 BASIC			3.55 BASIC			1.55 BASIC		

	BA			BB			BC		
A	MAX	NOM	MIN	MAX	NOM	MIN	MAX	NOM	MIN
	32.65	32.50	32.35	32.65	32.50	32.35	32.65	32.50	32.35
D1	3.90 BASIC			2.90 BASIC			4.90 BASIC		
D2	2.25 BASIC			3.25 BASIC			1.25 BASIC		
D3	2.55 BASIC			3.55 BASIC			1.55 BASIC		

	CA			CB			CC		
A	MAX	NOM	MIN	MAX	NOM	MIN	MAX	NOM	MIN
	21.65	21.50	21.35	21.65	21.50	21.35	21.65	21.50	21.35
D1	3.90 BASIC			2.90 BASIC			4.90 BASIC		
D2	2.25 BASIC			3.25 BASIC			1.25 BASIC		
D3	2.55 BASIC			3.55 BASIC			1.55 BASIC		

Figure 19 Right-angle NAND module voltage key and height variations

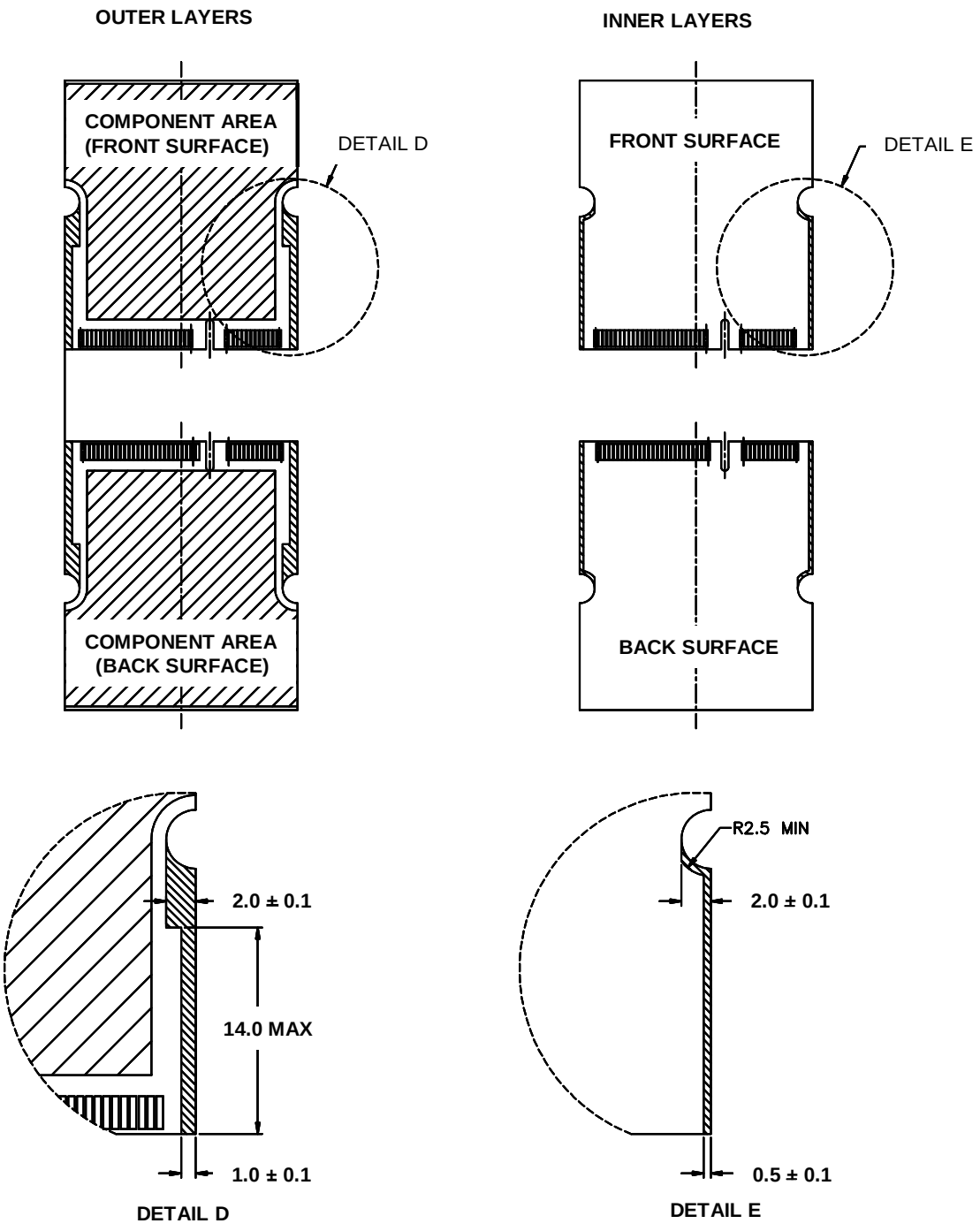


Figure 20 Right-angle NAND module non-metallization areas- Detail D and Detail E

4. Electrical Specification

This section specifies the NAND module connector electrical requirements including contact resistance, current carrying capacity, and the parasitic requirements.

4.1. DC Requirements

Table 4 outlines the NAND module connector DC electrical requirements, applicable to both the vertical and right angle connectors.

Parameter	Procedure	Requirements
Contact Resistance (LLCR)	EIA 364- 23B Subject mated contacts assembled in housing to 20 mV max open circuit at 100 mA max	Initial: 60 mΩ max for a mated connector Final (after stress): 80 mΩ max (allowable resistance change: 20 mΩ)
Current rating	EIA 364-70 method 2 Test the mated connector: 1. The sample size is a minimum of three mated connectors. 2. The sample shall be soldered on a PC board with the appropriate footprint. 3. Wire all the power and all the ground pins in a series circuit. 4. A thermocouple of 30 AWG or less shall be placed as close to the mating contact as possible. 5. Conduct a temperature rise vs. current test.	0.50 A per pin minimum. The temperature rise above ambient shall not exceed 30 °C. The ambient condition is still air at 25 °C.
Withstand Voltage	EIA364-20	500V min
Insulation Resistance	EIA364-21	1 MΩ min

Table 4 DC Electrical Requirements

4.2. Parasitic Requirements

Table 5 and Table 6 list the NAND module connector parasitic requirements for the vertical and right-angle NAND module connectors, respectively.

Parameter	Procedure	Requirements
C11: Signal-to-ground capacitance	See Appendix A	0.3-0.6 pF from 100 to 400 MHz
L11: Signal loop inductance	See Appendix A	2.5-3.5 nH from 100 to 400 MHz
C12: Coupling capacitance between adjacent signals	See Appendix A	0.3 pF max from 100 to 400 MHz
L12: Mutual inductance between adjacent signals	See Appendix A	0.9 nH max from 100 to 400 MHz
Note: The measurement does not include the connector through-hole, which is removed through calibration as discussed in Appendix A. The capacitance measurement does not include the module edge finger either.		

Table 5 Parasitic Requirements for the Vertical NAND Module Connector

Parameter	Procedure	Requirements
C11: Signal-to-ground capacitance	See Appendix A	0.7-2.0 pF from 100 to 400 MHz
L11: Signal loop inductance	See Appendix A	1.2-4.7 nH from 100 to 400 MHz
C12: Coupling capacitance between adjacent signals	See Appendix A	0.85 pF max from 100 to 400 MHz
L12: Mutual inductance between adjacent signals	See Appendix A	2.0 nH max from 100 to 400 MHz
Note: The measurement does not include the connector SMT pad, which is removed through calibration as discussed in Appendix A, but the measurement does include the module edge finger.		

Table 6 Parasitic Requirements for Right-angle NAND module Connector

5. Mechanical and Environmental Specification

This section specifies the NAND module connector mechanical and environmental requirements.

5.1. Mechanical Requirements

The mechanical requirements mainly include the mating force and durability. Table 7 lists the mechanical requirements.

Parameter	Procedure	Requirements
Mating force	EIA 364-13 Measure the force necessary to mate the connector assemblies at a max rate of 12.5 mm per minute.	55 N (12.4 lbf) max
Durability	EIA 364-09 25 cycles. Mate the connector as described in measuring mating force.	No physical damage to the connector. Meet requirements of additional tests as specified in the test sequence in Section 5.2.
Visual and dimensional inspection	EIA 364- 18 Visual, dimensional and functional inspection per applicable quality inspection plan.	Meets product drawing requirements
Lead-free soldering	No physical damage during lead-free soldering processes	Contact finish and header housing material be compatible with lead-free soldering process.

Table 7 NAND Module Connector (Vertical and Right-angle) Mechanical Requirements

5.2. Environmental Requirements

The NAND connectors shall meet the requirements for business office environment defined by EIA 364-1000.01. Follow EIA 364 1000.01 for environmental tests, using the following conditions:

- Durability (mating/unmating) rating of 25 cycles
- Temperature life test temperature and duration: 105 ^{o}C for 240 hours
- Temperature life test temperature and duration for preconditioning: 105 ^{o}C for 120 hours
- Mixed flowing gas test duration: 7 days (this is an optional test; connector vendors should work with their customers to decide if this is an appropriate test for the application)
- Maximum allowable LLCR change (between reading after stress and the initial reading): See Table 4.

APPENDIX A - Measurement of Connector Parasitics

A.1 Reference Equipment

The equipment referenced in the table below may be used for the connector parasitic measurements:

Equipment Name	Reference	Comment
Vector Network Analyzer (VNA) System	HP8720ES or equivalent	
Microprobes	40A-GS-1000-EDP and 40A-SG-1000-EDP from GGB)	From GGB for 0.5-1.0 mm pitch devices
Calibration Standard	CS-11 (The calibration standard is a high precision ceramic substrate that provides open, short, thru, and 50 Ω loads that can be used to calibrate out the effects of cables and probes)	From GGB
50 ohm Coax Cables	UFB197C	From Micro Coax

A.2 Test Fixture and Samples

Figure A1 describes details of the 4-layer DUT board. Figure A2 shows the DUT module PCB stackup to be used for the vertical connector; *the module PCB thickness shall be reduced to 1 mm for the right-angle connector*. The DUT board and DUT module impedance are defined as 50 (± 10%) ohms.

Figure A1 - DUT board PCB stackup

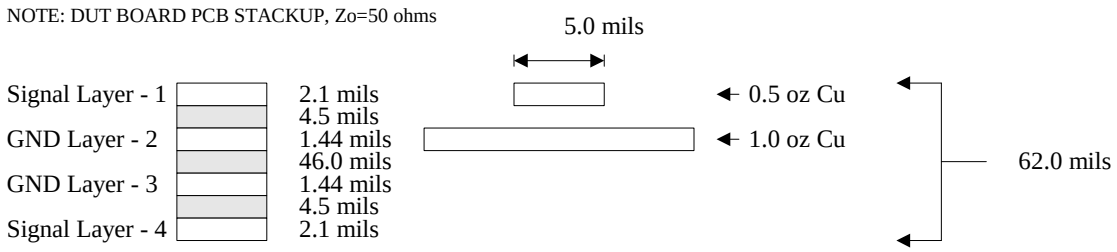
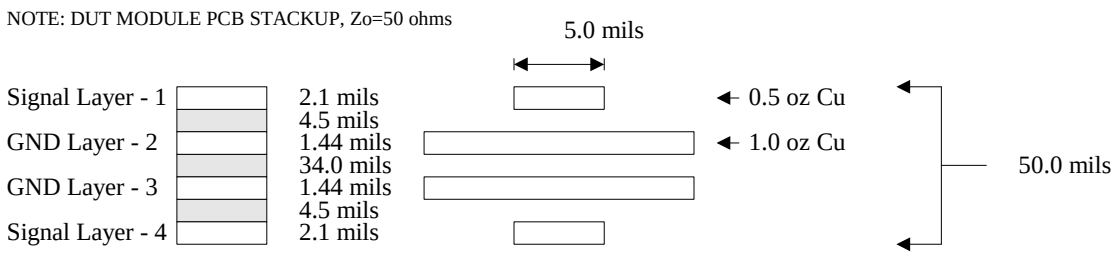
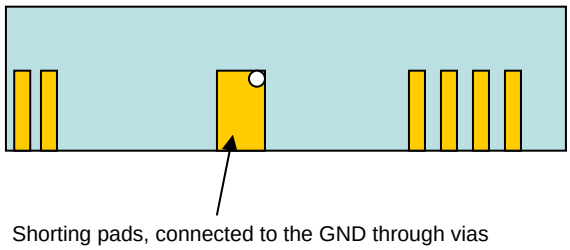


Figure A2 - DUT module PCB stackup For vertical connector



The DUT module is a printed circuit board with shorting and open pads. Figure A3 illustrates the DUT module with shorting pads.

Figure A3 - Short-circuit module card



A.3 Sample Preparation

DUT board and DUT module are for electrical test only.

For the through-hole connector: Align the connector pins with the corresponding through hole vias of the DUT board. Firmly press the connector into the board with uniform pressure across the connector body until all of the connector standoff points are flush with the DUT board surface. Use wave solder process to assemble the connector to the DUT board. Ensure that the gap between the DUT board and the connector standoff is less than 0.10 mm.

For the surface-mount connector: Solder the connector to the DUT board using a typical reflow process.

A.4 Network Analyzer Calibration

For all measurements, the DUT fixture must be calibrated so that device measurements do not include fixture inductance and capacitance parasitics of cables, probes, and the DUT board. These parasitic parameters need to be nulled out of the measured data. Obtain the calibration data of the probes from the supplier and enter the data into the "Calibration Kit" before performing the calibration.

A full two-port calibration is required before the measurement. The following is the recommended VNA setup:

Frequency	:	100 MHz-1000 MHz
Number of Points	:	801
Number of Averages	:	8
IF BW	:	300Hz

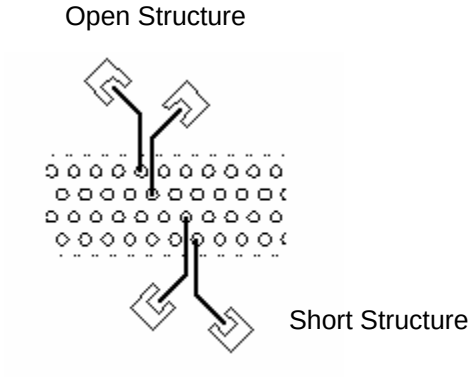
A.5 Measurement

A.5.1 DUT Board Parasitics

Figure A4 illustrates test points for calibration measurements. The contribution due to the DUT board must be calibrated out. The DUT board capacitance and inductance should be measured prior to soldering the connector to the DUT board.

The DUT board C_{11} and C_{12} measurements are to be made with open structures. Note that the pins used for capacitance measurement are open at the through-hole vias or the surface-mount pads. The two-port S-parameters can be measured from the open structures, and C_{11} and C_{12} can be derived from the measured S-parameters- See Section A.6. The averaged values from all the test points should be used as the DUT board capacitances.

Figure A4 – DUT board calibration structures



The DUT board L_{11} and L_{12} measurements are to be made with the short structures; the pins used for inductance measurement are short (to the ground plane) at the through-hole vias or the surface-mount pads. The two-port S-parameters can be measured from the short structures, and L_{11} and L_{12} can be derived from the measured S-parameters- See Section A.6. The averaged values from all the test points should be used as the DUT board inductances.

A.5.2 Connector Capacitance and Inductance

Measurements are to be done after the connector is soldered to the DUT board and the DUT board parasitic must be subtracted from the measurements to get the correct values.

To measure the capacitances for the vertical connector, the open connector shall be used with no DUT module being plugged into the connector. The measured two-port S-parameters can be converted to C11 and C12. Note that C11 and C12 are the total capacitance of the DUT board and the connector (not including the DUT module edge finger). The DUT board capacitance parasitic needs to be subtracted to get the connector capacitance, using the averaged values across all the test points. To measure the capacitance for the right-angle connector, the DUT module shall be plugged into the connector and the measurements shall be done at the test points that connect to open edge fingers on the DUT module.

To measure the inductance, the short-circuit test module is inserted into the connector slot and the short structures can be measured and averaged. Note that the inductance measured is the total inductance of both the DUT board and the connector. The DUT board inductance parasitic needs to be subtracted to get the connector inductance, using averaged values. The inductance value limits are applied to the average of all the test points.

A.6 Converting S-parameters to Parasitic

The measured 2-port S-parameters

$$[S]=\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \quad (1)$$

can be converted to the impedance (Z-) parameters:

$$[Z]=Z_o\cdot([I]+[S])\cdot([I]-[S])^{-1} \quad (2)$$

or the admittance (Y-) parameters:

$$[Y]=Z_0^{-1}([I]-[S])([I]+[S])^{-1}\cdot \quad (3)$$

where Z0=50 ohm, is the reference characteristic impedance and [I] is the 2x2 unit matrix.

The S-parameters from the open structures are used to extract capacitances via the admittance parameters:

$$C_{11}=\frac{1}{2}imag(Y_{11}+Y_{22})/\omega \quad (4)$$

$$C_{12}=\frac{1}{2}imag(Y_{12}+Y_{21})/\omega \quad (5)$$

where Y_{ij} (i,j=1,2) are the elements of [Y] and ω is the angular frequency.

The inductance can be extracted from the Z-parameters, obtained from the S-parameters of the short structures:

$$L_{11}=\frac{1}{2}imag(Z_{11}+Z_{22})/\omega \quad (6)$$

$$L_{12}=\frac{1}{2}imag(Z_{12}+Z_{21})/\omega \quad (7)$$

A.7 Report

Measurement results shall be reported in graphs, as illustrated in the figure below as an example.

Figure A4 – Illustration of an example of reporting C11 for the vertical connector