ONFI 2 Source Synchronous Interface Breaks the I/O Bottleneck

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Agenda

• NAND Flash performance bottlenecks
  ‣ I/O bottleneck
  ‣ Array architecture bottleneck
  ‣ Improving system performance

• ONFI 2 solves the I/O bottleneck
NAND – Performance Hasn't Increased with Density

Density / Performance

Time

DRAM

DRAM Density

DRAM Performance

NAND

NAND Density

NAND Performance
**Read Performance**

NAND array reads are parallel and very fast

- Read array bandwidth is greater than **330MB/s** (8KB read in 25us)

Interface speed is the limiting factor

- Read bus bandwidth is **40MB/s** (25ns clock)

Total throughput after array read and I/O transfer is **34MB/s**
Single Channel I/O Bottleneck

<table>
<thead>
<tr>
<th>Device</th>
<th>Planes</th>
<th>Data Size</th>
<th>Array Read (tR)</th>
<th>Data Output (tRC * Data Cycles)</th>
<th>Total Read Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLC 4KB page</td>
<td>2</td>
<td>8KB</td>
<td>25µs</td>
<td>211µs</td>
<td>34MB/s</td>
</tr>
<tr>
<td>MLC 4KB page</td>
<td>2</td>
<td>8KB</td>
<td>50µs</td>
<td>211µs</td>
<td>30MB/s</td>
</tr>
</tbody>
</table>

- Read performance is I/O limited because $t_{IO} \gg t_{R}$. 
Programming Performance

Interface speed is not the limiting factor

- Bus bandwidth is 40MB/s (25ns)
- Array program bandwidth is 33MB/s (8KB programmed in 250us)

Program performance is not so impressive

Total throughput after I/O transfer and array programming is 17MB/s
NAND Array Programming Bottleneck

<table>
<thead>
<tr>
<th>Device</th>
<th>Planes</th>
<th>Data Size</th>
<th>Data Input (tWC * Data Cycles)</th>
<th>Array Program (tPROG)</th>
<th>Total Write Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLC 4KB page</td>
<td>2</td>
<td>8KB</td>
<td>211µs</td>
<td>250µs</td>
<td>17MB/s</td>
</tr>
<tr>
<td>MLC 4KB page</td>
<td>2</td>
<td>8KB</td>
<td>211µs</td>
<td>900µs</td>
<td>7MB/s</td>
</tr>
</tbody>
</table>

- Program performance is array limited because tPROG ≫ tIO, especially for MLC devices.
Improving System Performance

- More die per channel

Controller

CE 0

NAND Flash

CE 1

NAND Flash

Controller

- More channels

NAND Flash

NAND Flash

NAND Flash

NAND Flash
Improving System Performance

- More die per channel *and* more channels
SLC 2-Plane Performance: Die per Channel vs. # of Channels

Read

Program

Performance (MB/s)

# of NAND Die per Channel

# of Channels
MLC 2-Plane Performance:
Die per Channel vs. # of Channels

Read

Program

Performance (MB/s)

# of NAND Die per Channel

# of Channels

MLC 2-Plane Performance:
Die per Channel vs. # of Channels

Read

Program

Performance (MB/s)

# of NAND Die per Channel

# of Channels
Pros and Cons

More Die per Channel

• Pros
  ‣ Low total pin count
  ‣ Low hardware cost to support

• Cons
  ‣ I/O-limited reads
  ‣ Eventually reach I/O-limited writes

More Channels

• Pros
  ‣ Scalable performance for reads and writes

• Cons
  ‣ Lots of pins on the host
  ‣ Expensive!
Agenda

- NAND Flash performance bottlenecks
  - I/O bottleneck
  - Array architecture bottleneck
  - Improving system performance

- ONFI 2 solves the I/O bottleneck
A Quick Introduction to the ONFI 2 Synchronous Interface

- The source synchronous interface defined in ONFI 2.0 increases the bandwidth of each I/O channel while adding only one pin, DQS
- ONFI 2.1 improves the I/O channel performance up to 200MB/s
- Designed for up to 16 die per I/O channel through use of output impedance control
- The protocol is backwards compatible to asynchronous NAND reducing or eliminating firmware changes for command set
- No DLL required in the NAND Flash devices
- May necessitate a new high-speed PHY, but was designed to be similar to mobile DRAM interfaces → evolutionary not revolutionary
- Because ONFI 2 devices are backwards compatible with the asynchronous NAND interface, controllers that only support the asynchronous interface can still use these devices
Legacy NAND ⇔ ONFI 2 Sync NAND Interface

Asynchronous NAND Interface Source Synchronous NAND Interface

- High-speed-capable NAND Flash devices power on using the asynchronous interface for backwards compatibility
- Set Features enables source synchronous interface
- WE# becomes a fast CLK
- RE# handles data direction by becoming W/R# (Write/Read#)
- I/O[7:0] renamed to DQ[7:0] (name change only, functionally identical)
- DQS, a new bi-directional signal, is enabled
Low Power Signaling

- As process geometry shrinks it becomes more difficult for controllers to stay with 3.3V I/O
  - Many applications today use 1.8V signaling
  - Many high-speed interfaces today use smaller voltage swings so signals can transition faster
    Example: Full-Speed USB – 12Mbit/s at 3.3V, High-Speed USB – 480Mbit/s at 400mV

- NAND Flash today requires the array and I/O to operate at the same voltage
  - $V_{cc} = 2.7-3.6V$, or
  - $V_{cc} = 1.7-1.95V$

- NAND Flash array operations perform best when $V_{cc} > 1.8V$ providing faster Program, Read, and Erase times

- By splitting the array voltage ($V_{cc}$) from the I/O voltage ($V_{ccQ}$) it is possible to get fast array operations and faster, lower power I/O signaling

- Possible ONFI 2 synchronous interface voltage configurations
  - $V_{cc} = 2.7-3.6V$, $V_{ccQ} = 2.7-3.6V$
  - $V_{cc} = 2.7-3.6V$, $V_{ccQ} = 1.7-1.95V$
High-Density Scalability

- By providing multiple output drive strength settings, many NAND devices can share the I/O bus while maintaining I/O throughput.

- Example: 133MB/s data throughput
  - 35-ohm driver, 4 NAND die
  - 25-ohm driver, 8 NAND die
  - 18-ohm driver, 16 NAND die
### Read Performance

**4 Gb Plane**

**330MB/s**

**4 Gb Plane**

**200MB/s**

**Shows significant improvement for single-die performance.**

**Shows significant gains for multiple die on the same channel.**

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<td>MLC 4KB page</td>
<td>2</td>
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<td>50µs</td>
<td>43µs</td>
<td>88MB/s</td>
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Programming Performance

Does not show much improvement for single-die performance.

Shows significant gains for multiple die on the same channel.

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Synchronous SLC 2-Plane Performance:
Die per Channel vs. # of Channels

Performance (MB/s)

# of Channels

# of NAND Die per Channel
Synchronous MLC 2-Plane Performance:
Die per Channel vs. # of Channels

Read

Program

Performance (MB/s)

# of NAND Die per Channel

# of Channels

# of Channels

Performance (MB/s)
Async vs. Sync SLC 2-Plane Performance: Die per Channel vs. # of Channels
Async vs. Sync MLC 2-Plane Performance: Die per Channel vs. # of Channels

Performance (MB/s)

# of NAND Die per Channel # of Channels

Read  Src  Sync  Read  Write  Src  Sync  Write
Conclusions

- ONFI 2 provides a significant increase to throughput per I/O channel
  - Allows better utilization of bus bandwidth
  - Requires less I/O channels overall
  - For read operations, a single die can immediately take advantage of higher bandwidth
  - For program operations, multiple die take advantage of higher bandwidth and reduce number of I/O channels required to achieve target bandwidths
For more information...

• Open NAND Flash Interface
  ‣ ONFI 2 specifications: http://www.onfi.org/
  ‣ ONFI 2 webinar: http://www.nand.com/

• Micron’s NAND Webinars:
  http://www.micron.com/products/nand/nand_webinars