Flash Performance Enhancements through ONFI

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Agenda

- Current state of NAND interoperability
- ONFI changes the paradigm
- History of Read performance enhancements
- High performance applications and utility of traditional Read performance enhancements
- How ONFI does it better
The State of NAND Interoperability

- NAND is the only commodity memory with no standard i/f
- Basic NAND commands are similar amongst vendors
  - Read, Program, Erase, Reset, Read Status
- Timings vary from vendor to vendor
  - Often supporting a few vendors easy, all is more difficult
- Enhanced NAND commands vary widely

![Diagram of NAND command timing and Read Cache protocols]
ONFI Paves the Way

- ONFI establishes a standard interface for NAND
  - A new paradigm is enabled: Host vendors no longer wait for the datasheet for the latest NAND part and then start making changes

- ONFI paves the way to:
  - Shorter NAND and product qualification times
  - More innovation since basic NAND command sequences always work
  - The host utilizing high performance command sequences

ONFI Founders
History of Read Performance Enhancements

- Cache Operations
  - Read Cache, variant 1
  - Read Cache, variant 2
- Multiple plane operations
  - Reads
Page Register Resource

- The page register is a critical data staging area in NAND operations

- Reads:
  1. Data flows from array to page register
  2. Data flows from page register to host

- Programs:
  1. Data flows from host to page register
  2. Data flows from page register to array

- The host is “stuck” until the page register is available again
Removing the Page Register Bottleneck

- While the host is reading data from the page register, the next page could be read from the array.
  But... there is only one page register...

- The NAND vendors added a cache register to solve this issue.
Read Cache, variant 1

- The sequence is:
  - Issue normal read command
  - Wait tR time
  - Then issue 31h command to tell the NAND to start a background read operation to the cache register

- Limitation:
  - Enhancement only applies for sequential page reads

![Diagram of READ BUS](image-url)
The sequence is:
- Issue a modified Read command; finish with 31h instead of 30h
- Each time the end of a page is reached, the NAND automatically starts reading the next page

Limitation:
- Enhancement only applies for sequential page reads
Multiple Plane Operations

- NAND vendors have started splitting the array into “planes” within a die

- Allows simultaneous operations of the same type to different block addresses
  - Reads
  - Programs
  - Erases
Multiple Plane Read Operations

- Multiple plane read operations are when multiple reads are issued at roughly the same time.

- Limitation:
  - Page address for reads have to be the same.

* Micron MT29F4G08AAA datasheet
Behavior of High Performance Applications

- Apps, like Robson, receive frequent random reads
- To achieve high read performance for high performance applications, handling random and non-deterministic read patterns well is required.
High Performance Apps and Read Enhancements

- Recall limitations with Read enhancements:
  - Read Cache: Must be sequential page within block
  - Multi-plane Reads: Needs to be same page in each block

- Recall high performance app read patterns:
  - Non-deterministic
  - Often highly random

Result: Traditional read enhancements have little value in high performance applications!
ONFI Simplifies while Expanding Utility

- ONFI defines one read enhancement
- Read Cache Enhanced
  - Allows 00h-Cmd 5-Address cycles to precede 31h of Read Cache (variant 1) to deliver a random read cache
  - Host can choose to issue 31h alone for sequential behavior, thereby preserving any previous host investment in Read Cache
ONFI Delivers Read Performance Benefits

- Read Cache Enhanced delivers dramatic performance benefits in any read sequence (sequential or random)
  - Typical SLC performance boosted by 30%+
  - Typical MLC performance boosted by 50%+

### Normal Page Read

<table>
<thead>
<tr>
<th>Page Read</th>
<th>READ time / Block (ns)</th>
<th>data /Block (byte)</th>
<th>Read Performance (MB/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLC</td>
<td>5,668,480</td>
<td>135,168</td>
<td>23.85</td>
</tr>
<tr>
<td>MLC</td>
<td>12,936,960</td>
<td>270,336</td>
<td>20.90</td>
</tr>
</tbody>
</table>

### Cache Read – Sequential Pages

<table>
<thead>
<tr>
<th>Read Cache Enhanced</th>
<th>READ time / Block (ns)</th>
<th>data /Block (byte)</th>
<th>Read Performance (MB/s) vs. Page Read (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLC</td>
<td>4,274,170</td>
<td>135,168</td>
<td>31.62 32.6%</td>
</tr>
<tr>
<td>MLC</td>
<td>8,533,710</td>
<td>270,336</td>
<td>31.68 51.6%</td>
</tr>
</tbody>
</table>

### Cache Read – Non-Sequential Pages

<table>
<thead>
<tr>
<th>Read Cache Enhanced</th>
<th>READ time / Block (ns)</th>
<th>data /Block (byte)</th>
<th>Read Performance (MB/s) vs. Page Read (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLC</td>
<td>4,285,570</td>
<td>135,168</td>
<td>31.54 32.3%</td>
</tr>
<tr>
<td>MLC</td>
<td>8,554,710</td>
<td>270,336</td>
<td>31.60 51.2%</td>
</tr>
</tbody>
</table>
ONFI Eliminates Interleaved Reads

- ONFI has chosen to not implement interleaved reads
  - Multiple plane operations map well to interleaved operations in ONFI

- Why?
  - Limitation of same page address makes utility low
  - Rife with bus contention issues
  - Read Cache Enhanced provides all of the benefits

**Step 1:** Array to Cache Register
20 microseconds (SLC)

**Step 2:** Page Register to Host
50 microseconds (25ns timings)

**Step 2** is the bottleneck. Reading more than one page in the background from the array is pointless. Still serialized to host...
Summary

- ONFI delivers standardized high performance command sequences that deliver real value
  - Simplifies numerous command sequences in the industry
  - Delivers value to high performance applications

- Join ONFI and help deliver more tangible benefits to the NAND industry