A Standard Interface for NAND Flash

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Agenda

System problems with NAND Today
NAND Flash Product Integration
Open NAND Flash Interface (ONFI) initiative overview
ONFI Technical Preview
System problems with NAND Today

NAND Flash Is Becoming a Commodity Memory Product

Total NAND Market Segment
(Billions of US$)

Source: WSTS, Micron Market Research
Intel’s NAND Dilemma...

NAND Flash is an increasingly important Intel platform ingredient

- Robson technology highlights increasing role of NAND Flash in Intel’s platform plans
- Intel’s platforms have longevity and address numerous market segments, which requires support for a range of NAND Flash components
- Intel’s stable platform must have the means for conveniently supporting the latest Flash components without having to be revamped

Current similar NAND Flash components do not allow for range of NAND to be accommodated in a platform
System problems with NAND Today

**Similar: Basic Commands**

Basic commands *typically* common

- Reset, Read ID, Read, Page Program, Erase, ...

More complex operations all over the map

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**Table 1. Command Sets**

<table>
<thead>
<tr>
<th>Function</th>
<th>1st. Cycle</th>
<th>2nd. Cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read</td>
<td>00h</td>
<td>30h</td>
</tr>
<tr>
<td>Read for Copy Back</td>
<td>00h</td>
<td>36h</td>
</tr>
<tr>
<td>Read ID</td>
<td>90h</td>
<td>-</td>
</tr>
<tr>
<td>Reset</td>
<td>FFh</td>
<td>-</td>
</tr>
<tr>
<td>Page Program</td>
<td>80h</td>
<td>10h</td>
</tr>
<tr>
<td>Cache Program</td>
<td>80h</td>
<td>16h</td>
</tr>
<tr>
<td>Copy-Back Program</td>
<td>85h</td>
<td>10h</td>
</tr>
<tr>
<td>Block Erase</td>
<td>60h</td>
<td>00h</td>
</tr>
<tr>
<td>Random Data Input*</td>
<td>85h</td>
<td>-</td>
</tr>
<tr>
<td>Random Data Output*</td>
<td>05h</td>
<td>C0h</td>
</tr>
<tr>
<td>Read Status</td>
<td>70h</td>
<td></td>
</tr>
</tbody>
</table>

---

*Samsung K9K4G08U0M datasheet

*Hynix HY27UG084G2M datasheet

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System problems with NAND Today

**Similar: Timing**

Timing requirements are specified differently
Min/max values are not necessarily the same for similar cycle time parts

*Samsung K9K4G08U0M datasheet

*Hynix HY27UG084G2M datasheet

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System problems with NAND Today

**Similar: Status Values**

Status values dependent on command
Often the same, but not required to be
–Can you tell that these are the same??

<table>
<thead>
<tr>
<th>I/O No.</th>
<th>Page Program</th>
<th>Block Erase</th>
<th>Cache Program</th>
<th>Read</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O 0</td>
<td>Pass/Fail</td>
<td>Pass/Fail</td>
<td>Pass/Fail(N)</td>
<td>Not use</td>
<td>Pass: '0' Fail: '1'</td>
</tr>
<tr>
<td>I/O 1</td>
<td>Not use</td>
<td>Not use</td>
<td>Pass/Fail(N-1)</td>
<td>Not use</td>
<td>Pass: '0' Fail: '1'</td>
</tr>
<tr>
<td>I/O 2</td>
<td>Not use</td>
<td>Not use</td>
<td>Not use</td>
<td>Not use</td>
<td>Don't care</td>
</tr>
<tr>
<td>I/O 3</td>
<td>Not Use</td>
<td>Not Use</td>
<td>Not Use</td>
<td>Not Use</td>
<td>Don't care</td>
</tr>
<tr>
<td>I/O 4</td>
<td>Not Use</td>
<td>Not Use</td>
<td>Not Use</td>
<td>Not Use</td>
<td>Don't care</td>
</tr>
<tr>
<td>I/O 5</td>
<td>Ready/Busy</td>
<td>Ready/Busy</td>
<td>True Ready/Busy</td>
<td>Ready/Busy</td>
<td>Busy: '0' Ready: '1'</td>
</tr>
<tr>
<td>I/O 6</td>
<td>Ready/Busy</td>
<td>Ready/Busy</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I/O 7</td>
<td>Write Protect</td>
<td>Write Protect</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Hynix HY27UG084G2M datasheet

*Samsung K9K4G08U0M datasheet

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System problems with NAND Today

Similar: Read ID

The first and second byte are consistently manufacturer and device ID

The number of remaining bytes and what they mean is up in the air

*Samsung K9K4G08U0M datasheet

<table>
<thead>
<tr>
<th>Description</th>
<th>I/O8</th>
<th>I/O7</th>
<th>I/O6</th>
<th>I/O5</th>
<th>I/O4</th>
<th>I/O3</th>
<th>I/O2</th>
<th>I/O1</th>
<th>Hex Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st Data</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maker Code</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>98H</td>
</tr>
<tr>
<td>2nd Data</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Device Code</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>DAH</td>
</tr>
<tr>
<td>3rd Data</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Chip Number, Cell Type,</td>
<td>0 or 1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>81H or 01H</td>
<td></td>
</tr>
<tr>
<td>PGM Page, Write Cache</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4th Data</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Page Size, Block Size,</td>
<td>0 or 1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>95H or 15H</td>
</tr>
<tr>
<td>Redundant Size, Organization</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5th Data</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Plane Number, Plane Size</td>
<td>0 or 1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>44H or C4H</td>
</tr>
</tbody>
</table>

*Toshiba TH58NVG1S3AFT05 datasheet

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System problems with NAND Today

**Similar Hinders NAND Adoption**

To deal with differences, the host must maintain a chip ID table of known devices

- Table contains read/write timings, organization, status bit meanings, etc for each known NAND Flash part

Situation has two major effects:

- Precludes intro of new NAND devices into existing designs
- Makes qualification cycles longer as each NAND device added requires changes to be comprehended

Similar to the ancient disk drive interfaces that required a list of disk drive types in a BIOS table

Lack of standard impacts platforms supporting a range of NAND
Agenda

- System problems with NAND Today
- NAND Flash Product Integration
- Open NAND Flash Interface (ONFI) initiative overview
- ONFI Technical Preview
Product Update Cycle for HDD

NAND Flash Product Integration

MP3 Player

HDD

30 GB

MP3 Player

HDD

60 GB

No software changes required
Product-level testing and validation focus
Physical and logical interface standard
Product Update Cycle for NAND

Firmware/software changes required
- Change device ID table to support new component
- Add support for new commands to maintain or increase performance

Potentially spin new Mask ROM (1 month delay)
Complete re-test of firmware and/or software
Inconsistency of NAND Flash

Higher Performance
- Parallel operations
- Faster timing

Higher Density
- (Multi-level cell) MLC
- Fewer erase cycles

Process Improvements
- 70nm, 55nm.....
Challenges for Controller

When new NAND Flash is released (from the same or a different vendor), the controller vendor needs to do numerous updates:

- Look for new Flash Device ID
- Update timing to comprehend new part
- Update ECC to comprehend bit rate
- Other modifications based on device parameters

Another challenge: these changes must be made to a Mask ROM, with small storage area (64KB typical) and updates requiring a 1 month wait for a new IC.

Controllers lag behind Flash updates, and is one of the last to know about changes...
NAND Flash Product Integration

Result of These Challenges

Inventory control is difficult and array of parts confusing to customers
- Mask ROMs are too small to support all Flash behavior, must choose subset
- Several firmware versions must be maintained for every controller to support most NAND in the market

Any firmware change results in one month delay to the customer
- Mask ROM change is 1 month for new IC
- In current environment, cannot anticipate any upcoming changes effectively
NAND Flash requires more qualification time than other commodity memory products
Lost revenue opportunity that could be rectified with standard interface

- Impossible today for controller to anticipate and be prepared for upcoming Flash behavior

Lack of standard interface impacts time to market and revenue
Agenda

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NAND Flash Product Integration
Open NAND Flash Interface (ONFI) initiative overview
ONFI Technical Preview
Open NAND Flash Interface (ONFI) initiative overview

Goals of Initiative:

To develop a standardized NAND Flash interface that allows interoperability between NAND devices

Accelerate time to market of NAND-based products
Technical Philosophy

ONFI shall ensure no pre-association with NAND Flash at host design is required
- Flash must self-describe features, capabilities, timings, etc, through a parameter page
- Features that cannot be self-described in a parameter page (like number of CE#) shall be host discoverable

ONFI should leverage existing Flash behavior to the extent possible
- Intent is to enable orderly and TTM transition, so highly divergent behavior from existing NAND undesired
- Where prudent for longevity or capability need, existing Flash behavior shall be modified or expanded

ONFI needs to enable future innovation
Open NAND Flash Interface (ONFI) initiative overview

Initiative Status

Intel is working with key partners to form the ONFI Workgroup
– More details to come imminently

ONFI specification expected to be released in 2H’06

ONFI is being developed to solve the barriers to the rapid adoption of new NAND products
Agenda

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ONFI Technical Preview
ONFI defines standard pin-outs for the 48-pin TSOP and 52-pin LGA packages

Pin-out critical for ensuring no board changes required in NAND Flash upgrade

- For example, the host can plan for a new part that will have an additional CE# beforehand
Fixing 16-bit Data Pin-out

The current industry x16 pin-out precludes board designs accepting both x8 and x16 parts easily

- The I/O0 – I/O7 pins are not in the same place!

ONFI is fixing this issue before x16 parts become entrenched (x16 currently is ~ < 1% of volume)
Device Abstraction

ONFI presents a device representation to the host based on independence “levels”
- ONFI has no notion of number of die or number of planes, etc.

Target: Completely independent unit with its own chip enable (CEx#)
- Logical Unit (LUN): Logically independent unit, shared chip enable
  - Interleaved Addressing: Dependent operations allowed for different blocks with same page address
Each target may support multiple logical units
Each LUN may support interleaved addressing for increased parallelism
Actual implementation abstracted

Target X, using CEx#
Determining ONFI Support

Read ID is used by Flash parts today to report device ID for use in chip ID table lookup.

ONFI support is shown by responding to Read ID for address 20h with ASCII ‘ONFI’

Support for vendor specific interface and ONFI allowed by changing address cycle to 20h from 0h.
Self Reporting Capabilities

Each target describes its features and capabilities through a parameter page.

Blocks of the parameter page are devoted to:

- Revision information
- Device features
- Manufacturer information
- Memory organization
- Timing parameters
- Vendor specific

Memory Organization Block of Parameter Page:

- Number of data bytes per page
- Number of redundant bytes per page
- Number of pages per block
- Number of blocks per logical unit (LUN)
- Number of logical units
- Number of address cycles
- Number of bits per cell
- Block endurance
- Number of programs per page
- Recommended bits of ECC correction
- Interleaved addressing
## Command Set Overview

<table>
<thead>
<tr>
<th>Command</th>
<th>O/M</th>
<th>1st Cycle</th>
<th>2nd Cycle</th>
<th>Acceptable while Accessed LUN is Busy</th>
<th>Acceptable while Other LUNs are Busy</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read</td>
<td>M</td>
<td>00h</td>
<td>30h</td>
<td></td>
<td>Y</td>
</tr>
<tr>
<td>Change Read Column</td>
<td>M</td>
<td>05h</td>
<td>E0h</td>
<td></td>
<td>Y</td>
</tr>
<tr>
<td>Change Read Column Enhanced</td>
<td>O</td>
<td>06h</td>
<td>E0h</td>
<td></td>
<td>Y</td>
</tr>
<tr>
<td>Read Cache</td>
<td>O</td>
<td>31h</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Read Cache End</td>
<td>O</td>
<td>3Fh</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Block Erase</td>
<td>M</td>
<td>60h</td>
<td>D0h</td>
<td></td>
<td>Y</td>
</tr>
<tr>
<td>Read Status</td>
<td>M</td>
<td>70h</td>
<td></td>
<td>Y</td>
<td></td>
</tr>
<tr>
<td>Read LUN Status</td>
<td>O</td>
<td>78h</td>
<td></td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Page Program</td>
<td>M</td>
<td>80h</td>
<td>10h</td>
<td></td>
<td>Y</td>
</tr>
<tr>
<td>Page Cache Program</td>
<td>O</td>
<td>80h</td>
<td>15h</td>
<td></td>
<td>Y</td>
</tr>
<tr>
<td>Change Write Column</td>
<td>M</td>
<td>85h</td>
<td></td>
<td></td>
<td>Y</td>
</tr>
<tr>
<td>Read ID</td>
<td>M</td>
<td>90h</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Read Parameter Page</td>
<td>M</td>
<td>ECh</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Get Features</td>
<td>O</td>
<td>E Eh</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Set Features</td>
<td>O</td>
<td>EFh</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reset</td>
<td>M</td>
<td>FFh</td>
<td></td>
<td>Y</td>
<td>Y</td>
</tr>
</tbody>
</table>
ONFI Technical Preview

Timing Requirements

NAND contains a lot of timing requirements and hence timings

Reporting each and every timing value leads to validation challenge

- Requires validation of all combinations

To make timing information useful, organized into timing modes

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>tADL</td>
<td>Minimum ALE to data loading time</td>
</tr>
<tr>
<td>tALH</td>
<td>Minimum ALE hold time</td>
</tr>
<tr>
<td>tALS</td>
<td>Minimum ALE setup time</td>
</tr>
<tr>
<td>tAR</td>
<td>Minimum ALE to RE# delay</td>
</tr>
<tr>
<td>tBERS</td>
<td>Maximum block erase time</td>
</tr>
<tr>
<td>tCEA</td>
<td>Maximum CE# access time</td>
</tr>
<tr>
<td>tCH</td>
<td>Minimum CE# hold time</td>
</tr>
<tr>
<td>tCHZ</td>
<td>Maximum CE# high to output hi-Z</td>
</tr>
<tr>
<td>tCLH</td>
<td>Minimum CLE hold time</td>
</tr>
<tr>
<td>tCLR</td>
<td>Minimum CLE to RE# delay</td>
</tr>
<tr>
<td>tREH</td>
<td>Minimum RE# high hold time</td>
</tr>
<tr>
<td>tRHOH</td>
<td>Minimum RE# high to output hold</td>
</tr>
<tr>
<td>tRHW</td>
<td>Minimum RE# high to WE# low</td>
</tr>
<tr>
<td>tRHZ</td>
<td>Maximum RE# high to output hi-Z</td>
</tr>
<tr>
<td>tRLOH</td>
<td>Minimum RE# low to output hold</td>
</tr>
<tr>
<td>tRP</td>
<td>Minimum RE# pulse width</td>
</tr>
<tr>
<td>tRR</td>
<td>Minimum Ready to RE# low</td>
</tr>
<tr>
<td>tRST</td>
<td>Maximum device reset time</td>
</tr>
<tr>
<td>tWB</td>
<td>Maximum WE# high to R/B# low</td>
</tr>
<tr>
<td>tWC</td>
<td>Minimum write cycle time</td>
</tr>
<tr>
<td>tWH</td>
<td>Minimum WE# high hold time</td>
</tr>
<tr>
<td>tWHR</td>
<td>Minimum WE# high to RE# low</td>
</tr>
<tr>
<td>tWP</td>
<td>Minimum WE# pulse width</td>
</tr>
</tbody>
</table>
Timing Modes

Timing modes define vast majority of required host timings as one “set”

Three parameters are specified separately in RPP

- Max page read time
- Max block erase time
- Max page program time

Timing modes supported reported in timing parameters block of RPP

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Mode Example</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min</td>
<td>Max</td>
<td></td>
</tr>
<tr>
<td>tADL</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>tALH</td>
<td>5</td>
<td>ns</td>
</tr>
<tr>
<td>tALS</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>tAR</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>tCEA</td>
<td>5</td>
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</tr>
<tr>
<td>tCH</td>
<td>10</td>
<td>ns</td>
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<td>tCHZ</td>
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<td>ns</td>
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<tr>
<td>tCLH</td>
<td>15</td>
<td>ns</td>
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<tr>
<td>tCLR</td>
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<td>...</td>
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<td>ns</td>
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<td>tWB</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>tWC</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>tWH</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>tWHR</td>
<td>60</td>
<td>ns</td>
</tr>
<tr>
<td>tWP</td>
<td>15</td>
<td>ns</td>
</tr>
</tbody>
</table>
Interleaved Operation

Interleaving may be used to complete the same operation on additional blocks on a per logical unit basis to enhance performance.
- Concurrent interleaving: Operations to all of the blocks is issued at the same time and then executes in parallel.
- Overlapped interleaving: Operations may be issued independently, allows host to determine later to do an additional operation.

Interleaved operations may be reads, programs, or erases.

When using interleaving, the lowest order bits of the block address may be modified.
- The rest of the address must be the same as the other operations being issued on that LUN.
Defect Mapping & Enumeration

An invalid block is indicated by a 00h value in the first or last page of a block

- Ensures robustness in marking bad pages in face of recoverable bit errors

The host uses this information to create its initial bad block table

```c
// For each LUN maps defects
for (i = 0; i < NumLUNs; i++) {

    // For each block within this LUN, map defects
    for (j = 0; j < BlocksPerLUN; j++) {
        Defective=FALSE;

        // If a 00h value is in the first page, this block is defective
        ReadPage(lun=i; block=j; page=0; DestBuff=Buff);
        for (column=0; column<PageSize+RedundantBytes; column++) {
            if (Buff[column] == 00h)
                Defective=TRUE;
        }

        // If a 00h value is in the last page, this block is defective
        ReadPage(lun=i; block=j; page=PagesPerBlock-1; DestBuff=Buff);
        for (column = 0; column < PageSize+RedundantBytes; column++) {
            if (Buff[column] == 00h)
                Defective=TRUE;
        }

        // If the block was defective, then keep track of this
        if (Defective)
            MarkBlockDefective(lun=i; block=j);
    }
}
```
ONFI support is identified via Read ID, the standard NAND chip ID command
NAND devices report their capabilities using the Read Parameter Page
ONFI standardizes the base subset of commands required to be supported by all NAND devices
ONFI supports increased performance through parallelism made possible by multiple LUNs and interleaved addressing
ONFI standardizes the pin-out and packaging to ensure no PCB changes are required for a new NAND part

ONFI provides the solid technical base necessary to confidently build NAND-based products
Summary

Lack of standard makes it impossible for platforms to support a range of NAND components, including components introduced at a later date.

Lack of standard NAND Flash interface impacts time to market and revenue.

ONFI is being developed to solve the barriers to the rapid adoption of new NAND products.

ONFI enables NAND feature self-identification, and standardizes command set, pin-out, and packaging.
Please fill out the Session Evaluation Form.

Additional sources of information on this topic:
Initiative updates available at: www.onfi.org

Session presentation available on IDF web site – when prompted enter:
Username: idf
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