Open NAND Flash Interface: The First Wave of NAND Standardization

Amber Huffman
Senior Staff Architect

MEMS 002
Agenda

• Problem ONFI solves
• Organization and current status
• Technical details
• What’s Ahead
Past, Present and Future NAND Flash Demand Drivers

- PC applications for NAND become a major demand driver starting with Robson in 2007

- PC Usages consume > 1,000 billion MB by 2010!
“Similar” Behavior among NAND Vendors

• To deal with differences, the host must maintain a chip ID table of known devices
Impact of “Similar” Behavior

- Differences impact time to market and revenue
  - Requires software/firmware updates and thus increases product qualification time

- NAND Flash requires more qualification time than other commodity memory products
- Lost revenue opportunity that could be rectified with standard interface

Differing implementations of NAND Flash interface impact time to market and revenue
NAND in Compute Platforms

• NAND is an increasingly important platform ingredient (like DRAM)

  - Intel’s platforms have longevity and address numerous market segments, which requires support for a range of NAND components.

  - Intel’s stable platform must have the means to easily support the latest Flash components.

Lack of standard impacts host ability to easily support a range of NAND devices
Agenda

• Problem ONFI solves
• Organization and current status
• Technical details
• What’s Ahead
Open NAND Flash Interface (ONFI)

- ONFI establishes a standard interface for NAND

- **New paradigm**: Host vendors can develop for features that they will support and enable them “on the fly” if the NAND supports it
  - Old paradigm: Host vendors wait for the latest NAND part and then start making changes to communicate with the base NAND

- ONFI paves the way to:
  - Shorter NAND and product qualification times
  - More innovation since NAND command sequences always work

*Other names and brands may be claimed as the property of others*
High Level Features in ONFI 1.0

• Discoverable capabilities
  – Provides parameter page that describes NAND capabilities

• Multiple LUN operations
  – Enables independent operations

• Interleaved operations
  – Enables operations of the same type to execute simultaneously on the same LUN

• Caching operations
  – Enables data transfer while array operations are ongoing

• Copyback for internal data moves

• Standard timing modes

<table>
<thead>
<tr>
<th>Command</th>
<th>O/M</th>
<th>1st Cycle</th>
<th>2nd Cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read</td>
<td>M</td>
<td>00h</td>
<td>30h</td>
</tr>
<tr>
<td>Copyback Read</td>
<td>O</td>
<td>00h</td>
<td>35h</td>
</tr>
<tr>
<td>Change Read Column</td>
<td>M</td>
<td>05h</td>
<td>E0h</td>
</tr>
<tr>
<td>Read Cache Enhanced</td>
<td>O</td>
<td>00h</td>
<td>31h</td>
</tr>
<tr>
<td>Read Cache</td>
<td>O</td>
<td>31h</td>
<td></td>
</tr>
<tr>
<td>Read Cache End</td>
<td>O</td>
<td>3Fh</td>
<td></td>
</tr>
<tr>
<td>Block Erase</td>
<td>M</td>
<td>60h</td>
<td>D0h</td>
</tr>
<tr>
<td>Interleaved</td>
<td>O</td>
<td></td>
<td>D1h</td>
</tr>
<tr>
<td>Read Status</td>
<td>M</td>
<td>70h</td>
<td></td>
</tr>
<tr>
<td>Read Status Enhanced</td>
<td>O</td>
<td>78h</td>
<td></td>
</tr>
<tr>
<td>Page Program</td>
<td>M</td>
<td>80h</td>
<td>10h</td>
</tr>
<tr>
<td>Interleaved</td>
<td>O</td>
<td></td>
<td>11h</td>
</tr>
<tr>
<td>Page Cache Program</td>
<td>O</td>
<td>80h</td>
<td>15h</td>
</tr>
<tr>
<td>Copyback Program</td>
<td>O</td>
<td>85h</td>
<td>11h</td>
</tr>
<tr>
<td>Change Write Column</td>
<td>M</td>
<td>85h</td>
<td></td>
</tr>
<tr>
<td>Read ID</td>
<td>M</td>
<td>90h</td>
<td></td>
</tr>
<tr>
<td>Read Parameter Page</td>
<td>M</td>
<td>ECh</td>
<td></td>
</tr>
<tr>
<td>Read Unique ID</td>
<td>O</td>
<td>EDh</td>
<td></td>
</tr>
<tr>
<td>Get Features</td>
<td>O</td>
<td>EEh</td>
<td></td>
</tr>
<tr>
<td>Set Features</td>
<td>O</td>
<td>EFh</td>
<td></td>
</tr>
<tr>
<td>Reset</td>
<td>M</td>
<td>FFh</td>
<td></td>
</tr>
</tbody>
</table>
ONFI 1.0 Status Update

- Workgroup has delivered 0.9 draft of the ONFI specification
- Final item to polish is the state machine describing ONFI behavioral requirements
  - Describes externally visible behavioral requirements between the host and the NAND

<table>
<thead>
<tr>
<th>L_Idle_TargetRequest</th>
<th>If Target indicates an address, the address is stored by the LUN.</th>
</tr>
</thead>
<tbody>
<tr>
<td>L_WP_Update</td>
<td>1. Target indicates WP# value</td>
</tr>
<tr>
<td>L_SR_Update</td>
<td>2. Target requests SR register update</td>
</tr>
<tr>
<td>L_Status_Execute</td>
<td>3. Target requests status or status command received</td>
</tr>
<tr>
<td>L_Idle_ClearPageReg</td>
<td>4. Target requests page register clear</td>
</tr>
<tr>
<td>L_Idle_InvalidPageReg</td>
<td>5. Target requests page register invalidate</td>
</tr>
<tr>
<td>L_PP_Execute</td>
<td>6. Target indicates Program request for this LUN</td>
</tr>
<tr>
<td>L_BE_WaitForCmd</td>
<td>7. Target indicates Erase request for this LUN</td>
</tr>
<tr>
<td>L_RD_WaitForCmd</td>
<td>8. Target indicates Read request for this LUN</td>
</tr>
<tr>
<td>L_Idle_RdUid</td>
<td>9. Target indicates Read Unique ID request</td>
</tr>
</tbody>
</table>

ONFI 1.0 specification to be published in January with full set of features
Agenda

• Problem ONFI solves
• Organization and current status
• **Technical details**
• What’s Ahead
Enhancing Read Performance

- The host cannot directly read from the NAND array
- Reads happen in two steps:
  - 1) Data flows from the array to the page register
  - 2) Data flows from the page register to the host
- NAND IHVs introduced a cache register to eliminate lock-step reliance on page register for multiple read commands
- Allows NAND to read the next page from the array while transferring the current page to the host

![Diagram showing the read process](image-url)
Read Cache command divergence

- In industry today, there are two Read Cache command variants in wide use

- Read Cache protocol 1:
  - Issue a modified Read command (finish with 31h instead of 30h)
  - Each time the end of a page is reached, the NAND automatically starts reading the next page

- Read Cache protocol 2:
  - Issue a normal read command and wait the \( t_R \) array access time
  - Issue a 31h command to tell the NAND to start a background read operation
Read Cache applicability to high performance applications

- Applications, like Robson, receive frequent small random reads
- Read Cache seems ideal for read sequence shown
- **Gotcha:** Read Cache is only for sequential access
- No address cycles provided for subsequent pages in either protocol

None of the reads are issued in sequential order.

No address cycles for next page.
ONFI delivers
Read Cache Enhanced

- ONFI enhances Read Cache to allow the host to specify the address for each cached read

- If no address provided, defaults to sequential access to preserve any previous host investment in Read Cache
Performance Benefit of Read Cache Enhanced

- Read Cache Enhanced delivers dramatic performance benefits in any read sequence (sequential or random)
  - For 25 ns I/O timings, benefit is 29.6%
  - For 20 ns I/O timings, benefit is 36.5%

- Benefit grows with faster I/O timings

<table>
<thead>
<tr>
<th></th>
<th>Read Performance, 25 ns I/O timings</th>
<th>Read Performance, 20 ns I/O timings</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal page read</td>
<td>28.94 MB/s</td>
<td>33.86 MB/s</td>
</tr>
<tr>
<td>Read Cache,</td>
<td>37.62 MB/s</td>
<td>46.34 MB/s</td>
</tr>
<tr>
<td>sequential</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Read Cache,</td>
<td>37.52 MB/s</td>
<td>46.22 MB/s</td>
</tr>
<tr>
<td>random</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Copyback for Data Moves

• Copyback is a common NAND command used to move data from one block to another
  – Example: Move page 1 in A to page 0 in B

• Used for relocations and other operations where the host does not need to read the data
  – Note: The host can modify the data in the page register
Data Integrity and Copyback

- Copyback does not allow the host to read the data.
- If there is an ECC error on the read from the original location, the error is **propagated**.
- Use of traditional copyback reduces data integrity.

No data output allowed
Using Integrated ECC to Resolve Data Integrity concern

• One approach to resolving the data integrity concern is to integrate ECC in the NAND for copyback operations
  – Increases read busy time by $t_{EXTRA}$ to allow ECC evaluation

• Issues:
  – ECC NAND uses may not suit host application (e.g. too weak)
  – Time to evaluate in NAND is very likely longer than the host to do the same job
  – Integrated ECC increases the NAND die area

---

Read Page with no ECC evaluation

\[ t_R \]

Data download

Read Page with Integrated ECC

\[ t_R \]

\[ t_{EXTRA} \]

Data download
ECC evaluation
Read after error corr.
Copyback in ONFI

- ONFI resolves concern by making data output a mandatory part of Copyback.
- Hosts that desire high data integrity can use ECC of their choice.

Data output starting at column address specified

Change Read Column followed by output

Traditional Copyback after “A”
Increasing Concurrency for NAND Array Operations

- NAND vendors have started splitting the array into “planes” within a die

- Allows simultaneous operations of the same type to different blocks
  - Reads
  - Programs
  - Erases
Interleaved Operations

- To avoid dependence on NAND implementation and allow innovation, ONFI abstracts out multi-plane operations

- Interleaved operations are dependent operations allowed for different blocks on a logical unit
  - Interleaved address is LSB bit(s) of the block address

- Interleaving “types”:
  - Concurrent interleaving: Array operations for all blocks start after final command and execute in parallel
  - Overlapped interleaving: Array operations are independent and start after the operation is issued
Interleaved Erase Operations

- Sequence for concurrent and overlapped interleaved erases identical
- Easily extensible to more interleaved addresses with additional 60h/D1h sequences

![Diagram showing CLE, WE, ALE, RE, IO0-7, and R/B# signals with annotations for busy time and erase completion.]

Short busy time, ~ 3 µs
High when all erases complete
Interleaved Program Operations

- ONFI standardizes subsequent program commands as 80h
  - Some multi-plane program operations have 81h
  - No value in 81h, 82h, 83h, etc since previous ending command cycle of 10h or 11h provides necessary context

- Allows host to generically support n-interleaved addresses
Interleaved and Multi-Plane Limitations impact on Reads

- Interleaved operations and multi-plane operations have a significant limitation
  - The page address is required to be the same

* Micron MT29F4G08AAA datasheet

*Other names and brands may be claimed as the property of others
ONFI does not support Interleaved Reads

- ONFI has chosen to not implement interleaved reads
- Why?
  - Limitation of same page address makes utility low
  - Rife with bus contention issues
  - Read Cache Enhanced provides all of the benefits

**Step 1:** Array to Cache Register
20 microseconds (SLC)

**Step 2:** Page Register to Host
50 microseconds (25 ns timings)

Step 2 is the bottleneck. Reading more than one page in the background from the array is pointless. Still serialized to host…
ONFI Technical Details Summary

• ONFI enhances Read Cache to provide value in all read sequences

• ONFI removes data integrity concerns from Copyback with ECC flexibility

• ONFI provides high performance interleaved operation sequences
  – Allows for concurrent or overlapped array operations with a single host sequence
  – Plans for n-interleaved operations for the future

ONFI simplifies command sequences while enhancing value
Agenda

- Problem ONFI solves
- Organization and current status
- Technical details
- What’s Ahead
Where is ONFI Going?

- Standardization for existing NAND protocol was the first phase of ONFI

- NAND has enormous opportunities for innovation, which the ONFI Workgroup is evaluating

- The following foils show a flavor of the potential topics ONFI may pursue moving forward
  - I/O buffer timing enhancements
  - NAND connection in the platform
  - Block Abstracted NAND
I/O Buffer Timing Enhancements

- NAND timing is not source synchronous, making it difficult for the host to latch the data cleanly at higher speeds.
- This difficulty is reflected in the slowdown in NAND timing improvements.
- Enhancements beyond “going faster” will need to be made to get good scaling.

40% faster

50 ns I/O timings

30 ns I/O timings

25 ns I/O timings

17% faster
NAND Connection in the Platform

• NAND is penetrating the PC platform

• There is not a standard connector to enable attachment of NAND in the PC
  – I.e., there is nothing like a DIMM for NAND
Block Abstracted NAND to enable Broader NAND Use

- NAND may have ECC or other management requirements that are beyond the host’s capabilities
- Block Abstracted NAND allows a controller to be inserted in the middle that abstracts some of the complexities of NAND

```
ONFI NAND (2-bit ECC)

ONFI NAND (4-bit ECC)

Host

ONFI Controller
(3 bit ECC)

Host

ONFI Controller
(3 bit ECC)

Block Abstracted Controller
(8-bit ECC)
```
Join ONFI to Help Drive Future Innovation

- The ONFI Workgroup will be firming up the ONFI feature roadmap in the next month

Join ONFI

Thank you for your interest in joining the ONFI Workgroup. Membership in the ONFI Workgroup is open to all companies. Benefits for participating companies include:

- Contribution to the ONFI specification development
- Participate on ONFI activity email reflectors
- Preview early revisions of ONFI specifications
- Invitations to member meetings and events

Join ONFI to deliver more tangible benefits in key areas to the NAND industry
Summary

• Lack of standard impacts host ability to easily support a range of NAND devices

• ONFI 1.0 specification to be published in January with full set of features

• ONFI simplifies command sequences while enhancing value

• Join ONFI to deliver more tangible benefits in key areas to the NAND industry

Join ONFI to catch the next wave of NAND standardization
Additional sources of information on this topic:

- MEMC001 Chalk talk
- More web based info: www.onfi.org
Please fill out the Session Evaluation Form

Session presentation available in Content Catalog on the IDF web site – when prompted enter:
Username: idf
Password: fall2006
(Please note these are case sensitive)

Thank You for your input, we use it to improve future Intel Developer Forums

Join us at the Spring 2007 IDF on March 20-22 in San Francisco!!