ONFI: Leading the Way to Higher NAND Performance

Amber Huffman
Principal Engineer
Intel Corporation

June 7, 2007
Agenda

- PC platform and need for a standard
- High speed and PC opportunity
- Other key ingredients for PC use of NAND
The PC is a Key Component of NAND Growth

- NAND growth is projected to be 140% YoY for 06/07
- Largest growth area is “Others”
  - More than 50% projected QoQ growth for Q3/Q4
- A key component of the “Others” category is PC uses

<table>
<thead>
<tr>
<th>Unit: in 1Gb E., Million units</th>
<th>Q307F</th>
<th>Q407F</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Shipment</td>
<td>Demand</td>
</tr>
<tr>
<td>Digital Still Cameras</td>
<td>26.8</td>
<td>697.9</td>
</tr>
<tr>
<td></td>
<td>13.7%</td>
<td>32.0%</td>
</tr>
<tr>
<td>Cell phones</td>
<td>271.7</td>
<td>880.2</td>
</tr>
<tr>
<td></td>
<td>7.0%</td>
<td>38.0%</td>
</tr>
<tr>
<td>USB Drives</td>
<td>35.1</td>
<td>615.2</td>
</tr>
<tr>
<td></td>
<td>14.8%</td>
<td>29.0%</td>
</tr>
<tr>
<td>Flash-based MP3/PMP</td>
<td>32.6</td>
<td>779.7</td>
</tr>
<tr>
<td></td>
<td>9.5%</td>
<td>32.0%</td>
</tr>
<tr>
<td>Other (DVs, Game)</td>
<td>359.6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>54.0%</td>
<td></td>
</tr>
<tr>
<td>Total NAND Flash Demand</td>
<td>3,309.0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>33.0%</td>
<td></td>
</tr>
</tbody>
</table>

Worldwide NAND Flash IC Output (M 1Gb)

Source: DRAMeXchange, 4/2007
NAND Interoperability Impacts Adoption in PC Platforms

• NAND has been the only commodity memory with no standard
  – Command set, timings, and pin-out are similar among vendors

• Intel® Turbo Memory highlights the increasing role of NAND
  – Platforms have longevity (3+ years) and address many market segments
  – Platforms need to conveniently support new NAND components without silicon or even software changes (due to WHQL recertification)

• Lacking a standard, NAND is ill-suited to the realities of the PC

Read Cache protocol variants
Open NAND Flash Interface (ONFI)

**ONFI 1.0 defines:**
- Uniform NAND electrical and protocol interface
  - Raw NAND component interface for embedded use
  - Includes timings, electricals, protocol
  - Standardized base command set
- Uniform mechanism for device to report its capabilities to the host

**ONFI 1.0 status:**
- ONFI Workgroup formed in May ’06
- Ratified specification in Dec ’06

ONFI Establishes the First Standard NAND Interface
<table>
<thead>
<tr>
<th>Members</th>
<th>Members</th>
<th>Members</th>
</tr>
</thead>
<tbody>
<tr>
<td>A-Data</td>
<td>Alcor Micro</td>
<td>Aleph One</td>
</tr>
<tr>
<td>Arasan Chip Systems</td>
<td>ATI</td>
<td>Avid Electronics</td>
</tr>
<tr>
<td>BitMicro</td>
<td>Biwin Technology</td>
<td>Cypress</td>
</tr>
<tr>
<td>DataFab Systems</td>
<td>DataIO</td>
<td>Denali</td>
</tr>
<tr>
<td>FCI</td>
<td>Foxconn</td>
<td>Fusion Media Tech</td>
</tr>
<tr>
<td>Genesys Logic</td>
<td>Hagiwara Sys-Com</td>
<td>Hitachi GST</td>
</tr>
<tr>
<td>HiperSem</td>
<td>InComm</td>
<td>Intelliprop</td>
</tr>
<tr>
<td>ITE Tech</td>
<td>Jinvani Systech</td>
<td>Kingston Technology</td>
</tr>
<tr>
<td>Marvell</td>
<td>Molex</td>
<td>NVidia</td>
</tr>
<tr>
<td>Orient Semiconductor</td>
<td>Powerchip Semi.</td>
<td>PQI</td>
</tr>
<tr>
<td>Qimonda</td>
<td>Seagate</td>
<td>Shenzhen Netcom</td>
</tr>
<tr>
<td>Sigmatel</td>
<td>Silicon Storage Tech</td>
<td>Silicon Motion</td>
</tr>
<tr>
<td>SimpleTech</td>
<td>Skymedi</td>
<td>Smart Modular Tech.</td>
</tr>
<tr>
<td>Telechips</td>
<td>Teradyne, Inc.</td>
<td>Testmetrix</td>
</tr>
<tr>
<td>Transcend Information</td>
<td>Tyco</td>
<td>UCA Technology</td>
</tr>
<tr>
<td>USBest Technology</td>
<td>WinBond</td>
<td></td>
</tr>
</tbody>
</table>

*ONFI Membership Continues to Grow*

*Other names and brands may be claimed as the property of others*
NAND Changes for ONFI Support

- ONFI 1.0 standardizes similar behavior of industry NAND

- Two NAND changes are needed to comply with ONFI 1.0

Modification 1
- Read ID indicates ONFI compliance

Modification 2
- Read Parameter Page describes NAND capabilities
  - Allows new NAND to be used in older hosts

- The host may choose whether or not to use these capabilities

ONFI 1.0 is Easy for the Industry to Adopt
Agenda

• PC platform and need for a standard
• High speed and PC opportunity
• Other key ingredients for PC use of NAND
NAND Performance is Limited by the Legacy Interface

• NAND performance is determined by two elements:
  – Array access time
  – Time to transfer data to/from the data buffer in the NAND

• For reads, the dominant factor is the transfer to the data buffer
  – Limits performance to 40 MB/s
  – Could achieve over 150 MB/s with interface improvements

• As page size increases, the interface bottleneck gets even larger

ONFI 2.0 is Solving the Interface Bottleneck
ONFI is Delivering Higher Speed

• ONFI is following a straight forward path to higher speed

  Step 1: Source synchronous
  – Add source synchronous data strobes

  Step 2: Learn from DRAM
  – Follow the lessons of DDR

  Step 3: Easy transition
  – Avoid change for change’s sake

ONFI Interface Rate Roadmap

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Legacy</td>
<td>40 MB/s</td>
</tr>
<tr>
<td>Gen1</td>
<td>~ 133 MB/s</td>
</tr>
<tr>
<td>Gen2</td>
<td>~ 266 MB/s</td>
</tr>
<tr>
<td>Gen3</td>
<td>400 MB/s +</td>
</tr>
</tbody>
</table>

ONFI is Leading the Way to 10x Higher Performance
Going Source Synchronous

- A source synchronous data strobe is added to indicate where data should be latched
  - ONFI adds one new signal for the first generation

- The write and read enable signals are re-purposed for high speed
  - Write enable is used as a clock for all data input, output
  - Read enable is used to indicate the direction of data transfer

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O[7:0]</td>
<td>DQ[7:0]</td>
<td>I/O</td>
</tr>
<tr>
<td>—</td>
<td>DQS</td>
<td>I/O</td>
</tr>
<tr>
<td>WE#</td>
<td>CLK</td>
<td>Input</td>
</tr>
<tr>
<td>RE#</td>
<td>W/R#</td>
<td>Input</td>
</tr>
</tbody>
</table>
Learning from DRAM

- High speed NAND uses a DDR protocol
  - DDR balances performance and power

- DQS identifies the start of a data byte on the DQ bus
  - Data is latched on each edge of DQS (rising and falling)
NAND Impact for a PC
Application Launch Workload

Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance of Intel products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance.

HDD baseline system

NVM enhanced system

Effective Data Rate for Flash Solution 7x Higher
Can higher speed NAND improve performance of this workload further?
Opportunity for High Speed Impact

Over 75% of Workload Time in NAND Data Transfer
Agenda

• PC platform and need for a standard
• High speed and PC opportunity
• Other key ingredients for PC use of NAND
Non-Volatile Memory Host Controller Interface

• An impediment to enabling NAND benefits broadly in the PC is the lack of a standard register programming interface
  - There is no standard driver interface that allows OS vendors to provide a base support for platform NAND solutions

• Industry leaders have formed the NVMHCI Workgroup to define a standard host controller interface
  - NVMHCI heavily leverages the Serial ATA AHCI interface for fast time to market, and to enable a single driver to manage SATA and a platform NVM device

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Microsoft PressPass - Information for Journalists

Dell, Intel and Microsoft Join Forces to Increase Adoption of NAND-Based Flash Memory in PC Platforms

Newly formed group to provide standard interface for nonvolatile memory subsystems.

REDMOND, Wash. — May 30, 2007 — Broad adoption of NAND flash memory technology in the PC platform received a boost with the formation of the Non-Volatile Memory Host Controller Interface (NVMHCI) Working Group. The NVMHCI Working Group is chaired by Intel Corporation with core contributors including Dell Inc. and Microsoft Corp.

Related Links
External Resources:
- Dell Web site
- Intel Web site
NAND in the Platform

- NAND in the platform has started with modules plugged in on PCIe

- As NAND becomes more prevalent, the controller will be integrated with the platform
  - Down on motherboard or higher levels of integration

- OEMs want to offer customers capacity/feature choice, so NAND will remain on a module

- **Issue:** How to plug a NAND-only module into a PC platform?
  - NAND does not talk PCIe*

*Note: This seems to be a typographical error as NAND controllers typically do communicate with PCIe. The asterisk might indicate an intended footnote or clarification that is not shown in the image.*
Connector for NAND-only Modules

- To offer capacity choice, ONFI is defining a standard connector
  - Enables OEMs to sell NAND on a module
  - Like an unbuffered/unregistered DIMM

- The ONFI connector effort is leveraging existing DRAM standards
  - Avoids major connector tooling costs
  - Re-uses electrical verification
  - Ensures low cost with quick time to market

- Both right-angle and vertical entry form factors are being delivered

Standard NAND-only Module Important as NAND Becomes a Critical Component of PC Platforms
Summary

• ONFI 1.0 defines a standard interface for NAND
  – More details at www.onfi.org

• ONFI 2.0 is defining a higher speed interface NAND
  – Multi-generation roadmap delivering up to 10x in performance
  – Performance delivers significant benefits in PC platform workloads

• Other key pieces for PC platform use of NAND include:
  – NVMHCl standard register programming interface
  – NAND-only module for continued up-sell and customer choice

ONFI is Leading the Way to Higher Performance – New Features Critical for PC Platform Use of NAND