ONFi 3.0: The Path to 400MT/s NAND Interface Speeds

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ONFi Workgroup produces results!

- ONFi has and continues to deliver innovation & interoperability enabling faster NAND adoption

### Major Revisions

<table>
<thead>
<tr>
<th>Spec Version</th>
<th>2H '06</th>
<th>1H '07</th>
<th>2H '07</th>
<th>1H '08</th>
<th>2H '08</th>
<th>1H '09</th>
<th>2H '09</th>
<th>1H '10</th>
<th>2H '10</th>
</tr>
</thead>
<tbody>
<tr>
<td>ONFi 1.0: Standard electrical &amp; protocol interface, including base command set</td>
<td>Block Abstracted NAND</td>
<td>ONFi 2.0: Defined a high speed DDR i/f, tripling the traditional NAND bus speed in common use</td>
<td>ONFi 2.1</td>
<td>ONFi 2.2</td>
<td>ONFi 2.3: EZ NAND</td>
<td>EZ NAND / ONFi 2.3: Enabled ECC / management offload option</td>
<td>ONFi 3.0: Scaled high speed DDR i/f to 400 MT/s</td>
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</tbody>
</table>

### Speed

<table>
<thead>
<tr>
<th>Industry</th>
<th>50 MB/s</th>
<th>133 MB/s</th>
<th>200 MB/s</th>
<th>400 MB/s</th>
</tr>
</thead>
</table>

**ONFi – JEDEC Collaboration**
JEDEC and the Open NAND Flash Interface Workgroup Collaborate on NAND Standardization Defining a Next-Generation NAND Standard with Global Reach

Arlington, VA - May 30, 2008 - JEDEC and The Open NAND Flash Interface Workgroup (ONFi) announced today that they have entered into a collaborative agreement under which they will work together to develop NAND flash specification(s). ONFi is submitting the ONFi 2.0 specification as part of this joint effort. The goal of this joint activity will be to unify the industry and develop a standard which is backward compatible with existing flash interface technologies, including ONFi 2.0.

• Goal of harmonizing ONFi and Toggle Mode
• 200 MT/s compatibility: command set, packaging, impedance, etc
  • This specification is ~6 months away
• 400 MT/s: Achieve compatibility for data interface. Specification will be actively developed after 200 MT/s specification is completed
ONFi 3.0 Overview

- ONFi 3.0 will enable speeds up to 400 MT/s
  - Differential signaling
  - Control signal reduction with Volume addressing
  - On Die Termination
  - Reduced input voltage requirements
  - External Vref
  - Maintain backwards compatibility
Achieving 400 MT/s

- Highly dependent on form factor and topology
  - How many devices per channel?
  - How many packages per channel?
  - Distance from host controller to NAND technology?
  - PCB trace widths and spacing

ONFi 3.0 MLC-based I/O speeds

Number of die on a single channel
- Cache read
- Cache program
Differential Signaling

- ONFi 3.0 adds differential signaling for DQS and RE
  - Independent enablement of RE and DQS
  - Immunity to GND noise
  - Immunity to Cross Talk
  - Small voltage swings reduce power
Discrete CE_n per package

CE_n Reduction

Santa Clara, CA
August 2010
Mechanism for Volume Appointment

- Simple Example of Volume addressing
  - Host appoints Volume address at initialization
Volume addressing

- Operation using volume addressing
  - CE_n is brought high and then low
  - Volume Select command is issued by host to select target volume
  - Non-target Volumes are deselected until next CE_n pulse followed by Volume Select command
- Volume interleaving can be used to improve performance
Benefits of On Die Termination

- ODT is a key enabler for 400 MT/s operation
  - RE, DQS, and DQ[7:0]
  - Data eye with and without termination at 400 MT/s

![Graphs showing data eye with and without termination at 400 MT/s](image_url)
On Die Termination

• Each LUN (die) may be the terminator for any volume
  • Terminator for its volume: Target termination
  • Terminator for another volume: Non-target termination
• At initialization, the LUN is configured with the volumes it will terminate for
  • This provides a very flexible termination matrix
• If Volume Select command is issued to a volume the LUN is the terminator for, it stays partially active and terminates when data is transferred

<table>
<thead>
<tr>
<th>Volume</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Volume Byte 0</td>
<td>VOL7</td>
<td>VOL6</td>
<td>VOL5</td>
<td>VOL4</td>
<td>VOL3</td>
<td>VOL2</td>
<td>VOL1</td>
<td>VOL0</td>
</tr>
<tr>
<td>Volume Byte 1</td>
<td>VOL15</td>
<td>VOL14</td>
<td>VOL13</td>
<td>VOL12</td>
<td>VOL11</td>
<td>VOL10</td>
<td>VOL9</td>
<td>VOL8</td>
</tr>
</tbody>
</table>

Matrix of Volumes that LUN may enable termination
Flexible Termination Matrix

NON-TARGET TERMINATION EXAMPLE
Flexible Termination Matrix

TARGET TERMINATION EXAMPLE
Flexible Termination Matrix

PARALLEL NON-TARGET TERMINATION EXAMPLE
Reduced Input Voltage Requirements

- **SSTL_18**
  - 400 MT/s only supported at 1.8V VccQ
  - Industry standard that is easily adaptable
  - Allows for higher speeds and lower power consumption

- **External Vref**
  - VccQ/2
  - Allows for tighter setups/holds due to controlled reference
  - Reduces effects from external GND bounce
Backwards Compatibility

• ONFi 3.0 adds “Enhanced” Sync DDR for up to 400 MT/s that is enabled with Set Features command

• “Conventional” Sync DDR up to 200 MT/s and Async interface are still supported.

• ONFi 3.0 features to reach 400 MT/s are designed to be enabled independently on a system required basis allowing system designer cost vs. performance flexibility.

• ONFi 3.0 is compatible with ONFi-JEDEC Joint Task Group standardization efforts
Summary

• ONFi 3.0 is coming soon!
  • ONFi will be published by the end of the year
  • Enabling 400 MT/s interface speeds
  • Features designed with flexibility for system designer
  • CE_n reduction for cost savings
  • Volume addressing for ODT flexibility