Simplify your NAND Design-In with ONFI

Join our workgroup of 100+ industry leaders dedicated to simplifying NAND Flash integration.

Onfi.org

The industry leaders in NAND standard definition since 2006


easy integration
full features
a shared platform of NAND innovation

Improving Interoperability with ONFI 3.1/3.2
- JEDEC and ONFI developed JESD230 packaging standard
- I/O speeds extended to 533 MT/s (ONFI 3.2)
- Industry-standard package types available

Enabling Lower Power and Higher Transfer Speeds with Future ONFI 4.0
- I/O speeds extended beyond 533 MT/s
- I/O switching levels reduced to 1.2V swings
- Continuity of industry-standard packages defined in ONFI 3.2
- Backward-compatible with ONFI 3.2

ONFI Features and Benefits

<table>
<thead>
<tr>
<th>Feature*</th>
<th>Benefit</th>
<th>ONFI 2.2/2.3</th>
<th>ONFI 3.1/3.2</th>
<th>ONFI 4.0 Preliminary</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standardized electrical specs and protocol</td>
<td>More consistency among vendors</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Simplified host discovery of NAND features</td>
<td>Eases burden on firmware to identify features based on manufacturer and device IDs</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Maximum transfer speed MT/s</td>
<td>Faster interface reduces data access time</td>
<td>50 DDR-200</td>
<td>50 DDR-200</td>
<td>DDR-400 (3.1) DDR-533 (3.2)</td>
</tr>
<tr>
<td>I/O signaling voltage</td>
<td>Lower I/O voltage means lower switching power</td>
<td>3.3V</td>
<td>1.8V/3.3V*</td>
<td>1.8V/3.3V*</td>
</tr>
<tr>
<td>Industry-standard packages</td>
<td>Drives high bandwidth with small form factors (4-channel BGA, ONFI 3.2)</td>
<td>TSOP LGA</td>
<td>TSOP BGA</td>
<td>TSOP LGA</td>
</tr>
<tr>
<td>Interface backwards compatibility</td>
<td>Enables fastest devices to be run using slower interfaces</td>
<td>SDR</td>
<td>SDR</td>
<td>SDR, NV-DDR</td>
</tr>
<tr>
<td>Improved power management with ability to stop the clock</td>
<td>Lowers power consumption</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Enhanced ECC reporting</td>
<td>Reports extended ECC correction details to host</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Interleaved reads of LUNs</td>
<td>Improves pipelined reads</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Small data move</td>
<td>Minimizes the SRAM required for lower-cost controllers</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Change row address command</td>
<td>Improves the ability to save host data fragments (short pages)</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Program clear (PC) parameter</td>
<td>Improves writes with interleaved reads on another LUN</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>ECC ZERO (EZ NAND™) interface</td>
<td>ECC and provides corrected data to host</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>System signal reduction</td>
<td>Combines some signals enabling fewer signals to be routed to the host</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Differential signaling</td>
<td>Improves signal integrity enabling faster speeds</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>On-die termination</td>
<td>Improves signal integrity enabling faster speeds</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>ZQ calibration</td>
<td>Output drive impedance variance improvement</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

*Contact vendor for specific supported features.  ❑ New in this version of the specification.
ONFI 3.2 NV-DDR2 Flash Performance

MLC Flash
16KB Page Performance*

Number of die per channel

<table>
<thead>
<tr>
<th>1</th>
<th>2</th>
<th>4</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>20 MB/s</td>
<td>41 MB/s</td>
<td>82 MB/s</td>
<td>164 MB/s</td>
</tr>
</tbody>
</table>

*Maximum sequential performance assuming no controller overhead

SLC Flash
16KB Page Performance*

Number of die per channel

<table>
<thead>
<tr>
<th>1</th>
<th>2</th>
<th>4</th>
<th>8</th>
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</thead>
<tbody>
<tr>
<td>73 MB/s</td>
<td>146 MB/s</td>
<td>291 MB/s</td>
<td>533 MB/s</td>
</tr>
</tbody>
</table>

*Maximum sequential performance assuming no controller overhead

Founders

Additional ONFI Members

AboUnion Technology
A-DATA
Alcor Micro
Aleph One
AMD
Apacer
Arasan Chip Systems
ASMedia Technology
Asolid Tech
Avid Electronics Corp
BitMicro
Biwin Technology
Blank Microsystems, Inc.
Cadence
Chipsbank
Cypress
DataFab Systems Inc.
Data I/O
Datallight, Inc.
Delkin Devices, Inc.
Densbits Technologies
Diablo Technologies
ENE Technology
Eonsil LLC
Entorlan Technologies
Evatronix
FCI
FormFactor, Inc
Foxconn
Fresco Logic
Fusion Media Tech
Genesys Logic
Hagiwara Sys-Com
HiperSem
HGST
Hyperstone
InCOM
Inphi Corp.
Integrated Device Technology, Inc.
IntelliProp Inc.
ITE Tech. Inc
JinVani Systech
Kingston Technology
Laron Technologies LLC
Lotes
LSI
Macronix International
Marvell
MemoCom Corp.
Mentor Graphics
Metaram
Moai Electronics Corp.
Mobile Semiconductor
Molex
NeoMagic Corporation
Nvidia
Orient Semiconductor Electronics
PACTron
Palmchip Corporation
PMC Sierra
Power Quotient International
Powerchip Semiconductor
Prolific Technology
Seagate
Shenzhen Netcom Electronics Co
Silicon Integrated Systems
Silicon Motion, Inc.
Silicon Storage Tech
STEC
Skymedi Corporation
Smart Modular Technologies
Solid State System Co
Super Talent Electronics
Synopsys
System Level Solutions, Inc.
Tandon
Tanisys
Telechips
Teradyne Inc.
Testmetrix
Transcend Information, Inc
TycoElectronics
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University of York
Viking Technology
Virident Systems
Western Digital
WinBond

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