400 MT/s NAND Interface Solutions

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Why 400 MT/s Interface Speeds?

- NAND architectures are moving toward larger data transfer sizes
- Increased bandwidth
  - High-performance computing applications
    - High-density SSDs
    - USB 3.0
- Reduced latency
400 MT/s NAND Interface Solutions

- ONFI 3.0 NV-DDR2
  - Released March 2011
  - ONFI 3.0 Webinar: micron.com/ONFI-3
- Toggle Mode 2.0
  - Announced July 2010
- Work occurring in JEDEC on 400 MT/s
- Reduced CIO
  - Removes features to reduce loading
Toggle Mode 2.0

- 400 MT/s DDR interface
  - Compatible with ONFI 3.0 NV-DDR2
- Differential signaling (RE and DQS)
- On-die termination
- External $V_{REFQ}$
- Reduced signaling (SSTL_18)
- Warm-up cycles
ONFI 3.0 NV-DDR2

- 400 MT/s DDR interface
  - Superset of Toggle Mode 2.0
- Differential signaling (RE and DQS)
- On-die termination
- External $V_{\text{REFQ}}$
- Reduced signaling (SSTL_18)
- Warm-up cycles
- Matrix on-die termination
- Volume addressing
Benefits of Termination

Chip in termination mode

To other circuitry such as RCV, ...
To achieve $R_{TT}$ of 50 ohms:

- $R_{TTPU} = 100$ ohms
- $R_{TTPD} = 100$ ohms

With $1.8V$ $V_{CCQ}$, each DQ draws $\sim 9mA$

For all terminated signals, this amounts to $\sim 160mW$ per channel to achieve 50 ohms termination with linear termination.
Matrix Termination vs. Self Termination

Self Termination

- Target only termination available
- If supported for reads, output drivers cannot be used for termination

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Matrix Termination vs. Self Termination

- Target or non-target termination capable
- Supported for reads and writes
Matrix Termination vs. Self Termination

Matrix Termination Non-Target

Target LUN

CE0_n

Data Channel

LUN 0
LUN 1

LUN 0
LUN 1

- Multiple LUNs can be terminators, providing a flexible array of termination values and locations

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• With heavy loading and long trace lengths, slew rates can become very slow.
Topology Considerations
Revisit Micron’s FMS 2011 presentations at:
www.micron.com/fms