How ONFI Standards are Fueling High-Performance SSDs

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ONFI Specification History

- ONFI formed May 2006
- ONFI 1.0 release December 2006
- ONFI 2.0 release February 2008
- ONFI 2.1 release January 2009
- ONFI 2.2 release October 2009
- ONFI 2.3 release August 2010
- ONFI 3.0 release March 2011
- ONFI 3.1 coming soon
- ONFI 4.0 under development
ONFI 3.0 NV-DDR2

- 400 MT/s DDR interface
  - Superset of Toggle Mode 2.0
- Differential signaling (RE and DQS)
- On Die Termination
- External VrefQ
- Reduced signaling (SSTL_18)
- Warm up cycles
- Matrix On Die Termination
- Volume Addressing
The ONFI 3.0 Advantage: Reduced Read Latency
The ONFI 3.0 Advantage: Sequential Performance

MLC Flash
16K Page Performance*

- Number of die per channel:
  - 1: 400 MB/s, 21 MB/s
  - 2: 400 MB/s, 42 MB/s
  - 4: 400 MB/s, 85 MB/s
  - 8: 400 MB/s, 170 MB/s

SLC Flash
16K Page Performance*

- Number of die per channel:
  - 1: 400 MB/s, 73 MB/s
  - 2: 400 MB/s, 147 MB/s
  - 4: 400 MB/s, 291 MB/s
  - 8: 400 MB/s

*Maximum sequential performance assuming no controller overhead.
The ONFI 3.0 Advantage: SSD Performance

![Bar chart showing percentage change in IOPs versus NAND I/O transfer rate (MT/s).]
ONFI 3.0 Adoption Update

- Multiple vendors have controllers or IP blocks that are capable of enabling ONFI 3.0 NAND
  - See many of these products at the ONFI booth
- Micron has NV-DDR2 capable devices available for sampling
  - 20nm 128Gb monolithic
ONFI 3.1 To Be Released Soon

Performance & Feature Enhancements Continue

• LUN Get/Set Feature commands

• Relaxed NAND timing budget allotment
  • Support different data setup and hold values and still achieve same data input frequency
  • Provides support of the diverse usage of NAND devices for which the NV-DDR2 interface is used

• Multiple ECNs incorporated
ONFI 3.1 LUN Get/Set Feature

LUN Get Feature

LUN Set Feature
ONFI 3.0/3.1 400 MT/s timing budget
1V/nS input slew rate

ONFI 3.0/3.1 400 MT/s timing budget
0.3V/nS input slew rate
“Tight” timings

ONFI 3.1 400 MT/s timing budget
0.5V/nS input slew rate
“Tight” timings

ONFI 3.1 400 MT/s timing budget
0.5V/nS input slew rate
“Relaxed” timings
JC42.4 ONFI/JEDEC Joint Task Group

- Published specification that begins the process of interoperability between ONFI and Toggle Mode
  - Packaging
- Continuing work toward interoperability with new quarterly additions to the existing published specification
  - Next up Command Set
Future Activity

• Future ONFI 3.x specifications
  • Packaging
• ONFI 4.0 will focus on faster interfaces and lower power
• ONFI Industry Workgroup continues to advance NAND interface standards to enable higher performance NAND applications