JEDEC STANDARD

NAND Flash Interface Interoperability

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NAND Flash Interface Interoperability Standard

(From JEDEC BoD Ballot JCB-12-35 and JCB-12-52, formulatd under the cognizance of the JC-42.4 Subcommittee on DRAM Functions and Features.)

1 Scope

This document defines a standard NAND flash device interface interoperability standard that provides means for a system to be designed that can support Asynchronous SDR, Synchronous DDR and Toggle DDR NAND flash devices that are interoperable between JEDEC and ONFI member implementations. This standard was jointly developed by JEDEC and the Open NAND Flash Interface Wokrgroup, hereafter referred to as ONFI.

2 Terms, definitions, abbreviations and conventions

address: A character or group of characters that identifies a register, a particular part of storage, or some other data source or destination. (Ref. ANSI X3.172 and JESD88.)

NOTE 1 In a non-volatile memory array, the address consists of characters, typically hexadecimal, to identify the row and column location of the memory cell(s).

NOTE 2 For NAND non-volatile memory devices, the row address is for a page, block, or logical unit number (LUN); the column address is for the byte or word within a page.

NOTE 3 The least significant bit of the column address is zero for the source synchronous data interface.

asynchronous: Describing operation in which the timing is not controlled by a clock.

NOTE 1 For a NAND non-volatile memory, asynchronous also means when data is latched with the WE_n signal for the write operation and the RE_n signal for the read operation.

block: A continuous range of memory addresses. (Ref. IEC 748-2 and JESD88.)

NOTE 1 The number of addresses included in the range is frequently equal to 2n, where n is the number of bits in the address.

NOTE 2 For non-volatile memories, a block consists of multiple pages and is the smallest addressable memory segment within a memory device for the erase operation.

column: In a non-volatile memory array, a series of memory cells whose sources and/or drains are connected via a bit line.

NOTE 1 Depending on the non-volatile memory array, the bit line is accessed via the column select transistor, the column address decoder, or other decoding scheme.

NOTE 2 In non-volatile memory devices, a column decoder accesses a bit (x1), byte (x8), word (x16), or Dword (x32) either individually or within a page.

NOTE 3 In a typical schematic of a memory array, the column is in the vertical direction.

2 Terms, definitions, abbreviations and conventions (cont'd)

Dword (x32): A sequence of 32 bits that is stored, addressed, transmitted, and operated on as a unit within a computing system.

NOTE 1 A Dword may be represented as 32 bits, as two adjacent words, or as four adjacent bytes. When shown as bits, the least significant bit is bit 0 and the most significant bit is bit 31; the most significant bit is shown on the left. When shown as words, the least significant word (lower) is word 0 and the most significant (upper) word is word 1. When shown as bytes, the least significant byte is byte 0 and the most significant byte is byte 3.

NOTE 2 See Figure 1 for a description of the relationship between bytes, words, and Dwords.

latching edge: The rising or falling edge of a waveform that initiates a latch operation.

NOTE 1 For a NAND non-volatile memory the latching edge is the edge of the CK or DQS signal on which the contents of the data bus are latched for the source synchronous data interface.

NOTE 2 For a NAND non-volatile data cycles, the latching edge is both the rising and falling edges of the DQS signal.

NOTE 3 For a NAND non-volatile command and address cycles, the latching edge for the source synchronous interface is the rising edge of the CK signal.

NAND Defect Area: A portion of either first page and/or last page of factory marked defect block, and the defect area per page is defined as (# of data bytes) to (# of data bytes + # of spare bytes -1).

NOTE 1 For 8-bit data access NAND, the manufacturer shall set the first byte in the defect area, of the first or last page of the defect block to a value of 00h.

NOTE 2 For 16-bit data access NAND, the manufacturer shall set the first word in the defect area, of first or last page of the defect block to a value of 0000h.

NAND non-volatile memory device: The packaged NAND non-volatile memory unit containing one or more NAND Targets. Referred to as "device" in this publication.

NAND row address: Refers to the LUN, block and page to be accessed.

NOTE 1 The page address uses the least significant row address bits.

NOTE 2 The block address uses the middle row address bits.

NOTE 3 The LUN address uses the most significant row address bits.

page: The smallest non-volatile memory array segment, within a device, that can be addressed for read or program operations.

page register: A register used to transfer data from a page in the memory array for a read operation or to transfer data to a page in the memory array for a program operation.

read request: For NAND non-volatile memory a read request is a data output cycle request from the host that results in a data transfer from the device to the host.

2 Terms, definitions, abbreviations and conventions (cont'd)

source synchronous: For NAND non-volatile memory source synchronous describes the operation in which the strobe signal (DQS) is transmitted with the data to indicate when the data should be latched.

NOTE 1 The strobe signal (DQS) is similar in concept to an additional data bus bit.

target: A non-volatile memory component with a unique chip enable (CE_n) select pin.

word (x16): A sequence of 16 bits that is stored, addressed, transmitted, and operated on as a unit within a computing system.

NOTE 1 A word may be represented as 16 bits or as two adjacent words. When shown as bits, the least significant bit is bit 0 and the most significant bit is bit 15; the most significant bit is shown on the left. When shown as bytes, the least significant byte (lower) is byte 0 and the most significant byte is byte 2.

NOTE 2 See Figure 1 for a description of the relationship between bytes, words, and Dwords.

2.1 Abbreviations

DDR: Acronym for "double data rate".

LUN (logical unit number): The minimum memory array size that can independently execute commands and report status.

N/A: not applicable. Fields marked as "na" are not used.

O/M: Optional/Mandatory requirement. When the entry is set to "M", the item is mandatory. When the entry is set to "O", the item is optional.

status register (SR[x]): A register within a particular LUN containing status information about that LUN.

NOTE 1 SR[x] refers to bit "x" within the status register.

2.2 Conventions

2.2.1 Active-low signals

While the preferred method for indicating a signal that is active when low is to use the over-bar as in $\overline{CE}$, the difficulty in producing this format has resulted in several alternatives meant to be equivalents. These are the use of a CE reverse solidus (\ ) or the trailing underscore (_) following the signal name as in CE\ and CE_. In this publication "_n" is used to indicate an active low signal (i.e., an inverted logic sense).

2.2.2 Signal names

The names of abbreviations, initials, and acronyms used as signal names are in all uppercase (e.g., CE_n). Fields containing only one bit are usually referred to as the "name bit" instead of the "name field". Numerical fields are unsigned unless otherwise indicated.

2.2 Conventions (cont'd)

2.2.3 Precedence in case of conflict

If there is a conflict between text, figures, state machines, timing diagrams, and/or tables, the precedence shall be state machine, timing diagrams, tables, figures, and text.

2.3 Keywords

Several keywords are used to differentiate between different levels of requirements or suggestions.

mandatory: A keyword indicating items to be implemented as defined by a standard. Users are required to implement all such mandatory requirements to ensure interoperability with other products that conform to the standard.

may: A keyword that indicates flexibility of choice between stated alternatives or possibly nothing with no implied preference.

optional: A keyword that describes features that are not required by the specification. However, if any optional feature defined by the specification is implemented, that feature shall be implemented in the way defined by the specification.

reserved: A keyword indicating reserved bits, bytes, words, fields, and opcode values that are set-aside for future standardization. Their use and interpretation may be specified by future extensions to this or other specifications. A reserved bit, byte, word, or field may be cleared to zero or in accordance with a future extension to this publication. A host should not read/use reserved information.

shall: A keyword indicating a mandatory requirement.

should: A keyword indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase "it is recommended".

2.4 Byte, Word and Dword Relationships

Figure 1 Illustrates the relationship between bytes, words and Dwords

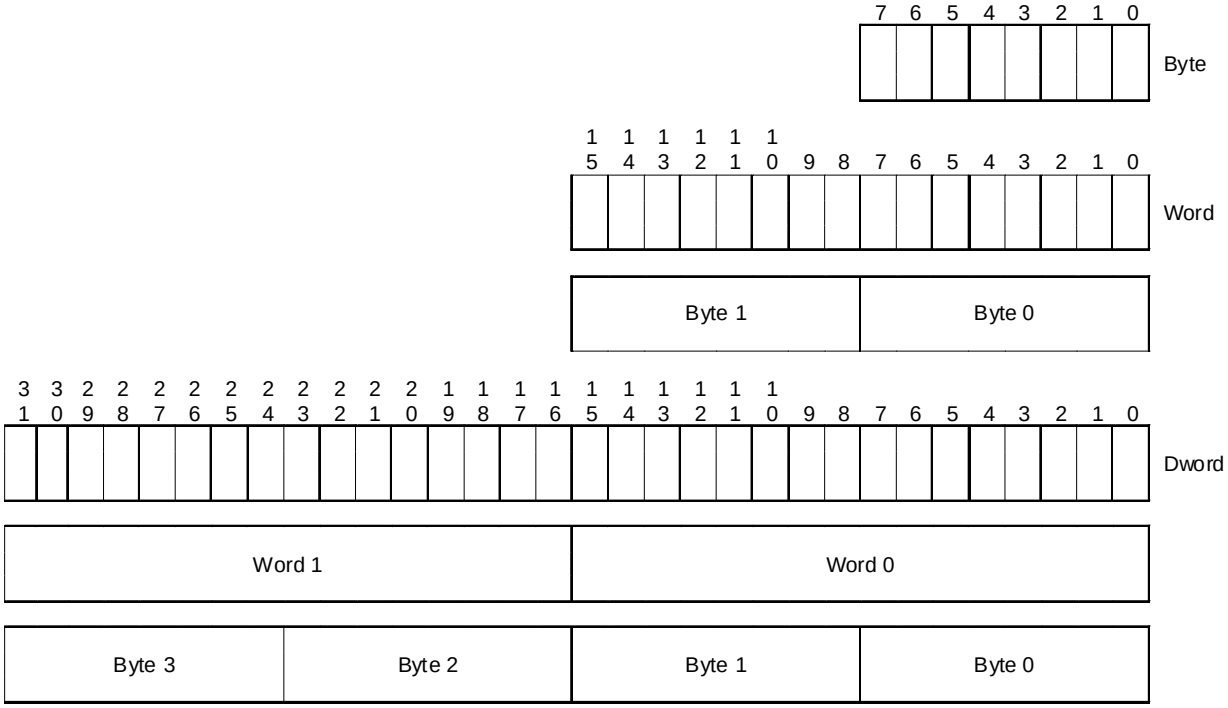

Figure 1 — Byte, word and Dword relationships

2.5 Signal description

Table 1 — Signal description

Name	Input/Output	Description
IO0 ~ IO7(~ IO15) DQ0 ~ DQ7	I/O	DATA INPUTS/OUTPUTS These signals are used to input command, address and data, and to output data during read operations. The signals float to high-z when the chip is deselected or when the outputs are disabled. IO0 ~ IO15 are used in a 16-bit wide target configuration. With multi channel support, IO0_0~IO7_0 and IO0_1~IO7_1 are used for IOs of channel 0 and IOs of channel 1 respectively. Also known as DQ0~DQ7 for Toggle DDR and Synchronous DDR.
CLE_x	I	COMMAND LATCH ENABLE The CLE_x signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data).
ALE_x	I	ADDRESS LATCH ENABLE The ALE_x signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data).
CE_x_n	I	CHIP ENABLE The CE_x_n input is the target selection control. When CE_x_n is high and the target is in the ready state, the target goes into a low-power standby state. When CE_x_n is low, the target is selected.
WE_x_n	I	WRITE ENABLE The WE_x_n input controls writes to the I/O port. For Asynchronous SDR Data, commands, addresses are latched on the rising edge of the WE_x_n pulse. For Toggle DDR commands, addresses are latched on the rising edge of the WE_x_n pulse.
R/B_x_n	O	READY/BUSY OUTPUT The R/B_x_n output indicates the status of the target operation. When low, it indicates that one or more operations are in progress and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
RE_x_n (RE_x_t)	I	READ ENABLE The RE_x_n input is the serial data-out control. For Asynchronous SDR Data is valid tREA after the falling edge and for Toggle DDR Data is valid after the falling edge & rising edge of RE_x_n which also increments the internal column address counter by each one.
RE_x_c	I	Complement of Read Enable This is the complementary signal to Read Enable
DQS_x (DQS_x_t)	I/O	Data Strobe The data strobe signal that indicates the data valid window for Toggle DDR and Synchronous DDR data interface. Output with read data, input with write data. Edge-aligned with read data, centered in write data.
DQS_x_c	I/O	Complement of Data strobe This is the complementary signal to Data Strobe.
W/R_x	I	Write/Read Direction The Write/Read Direction signal indicates the owner of the DQ bus and DQS signal in the Synchronous DDR data interface. This signal shares the same pin as RE_x_n in the asynchronous data interface.

CK_x	I	Clock The Clock signal is used as the clock in Synchronous DDR data interface. This signal shares the same pin as WE_x_n in the asynchronous data interface.
WP_x_n	I	WRITE PROTECT The WP_x_n disables the Flash array program and erase operations.
Vcc	I	POWER VCC is the power supply for device.
VccQ	I	I/O POWER The VccQ is the power supply for input and/or output signals.
Vss	I	GROUND The Vss signal is the power supply ground.
VssQ	I	I/O GROUND The VssQ signal is the ground for input and/or output signals
VSP	n/a	Vendor Specific The function of these signals is defined and specified by the NAND vendor. Any VSP signal not used by the NAND vendor shall not be connected internal to the device.
VREFQ	n/a	Reference voltage This is used as an external voltage reference.
ENi / ENo	I/O	Enumeration pins These pins may be used for ONFI NAND
R	n/a	Reserved These pins shall not be connected by host.
RFU	n/a	Reserved For Future use These pins may be assigned for certain functions in the future
NU	n/a	Not Usable A pin that is not to be used in normal applications and that may or may not have an internal connection.
NC	n/a	No (internal) connection A pin that has no internal connection and that can be used as a support for external wiring without disturbing the function of the device, provided that the voltage applied to this terminal (by means of wiring) does not exceed the highest supply voltage rating of the circuit.

3 Package and Addressing

3.1 BGA-63 (Single x8 / x16 BGA)

Figure 2 defines the ball assignments for devices using NAND Single x8 / x16 BGA packaging with 8-bit data access for the asynchronous SDR data interface. Figure 3 defines the ball assignments for devices using NAND Single x8 / x16 BGA packaging with 8-bit data access for the synchronous DDR data interface. Figure 4 defines the ball assignments for devices using NAND Single x8 / x16 BGA packaging with 16-bit data access for the asynchronous SDR data interface. The NAND Single x8/x16 BGA package with 16-bit data access does not support the Synchronous DDR data interface.

This package uses MO-201

	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC								NC	NC
C			WP_n	ALE	VSS	CE0_n	WE_n	R/B0_n		
D			VCC	RE_n	CLE	CE1_n	CE2_n	R/B1_n		
E			NC	NC	NC	NC	CE3_n	R/B2_n		
F			NC	NC	NC	NC	VSS	R/B3_n		
G			VSP3	VCC	VSP1	NC	NC	VSP2		
H			NC	IO0	NC	NC	NC	VCCQ		
J			NC	IO1	NC	VCCQ	IO5	IO7		
K			VSSQ	IO2	IO3	IO4	IO6	VSSQ		
L	NC	NC							NC	NC
M	NC	NC							NC	NC

Figure 2 — Ball assignments for 8-bit data access, asynchronous SDR only data interface

3.1 BGA-63 (Single x8 / x16 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC								NC	NC
C			WP_n	ALE	VSS	CE0_n	NC	R/B0_n		
D			VCC	W/R_n or RE_0_n	CLE	CE1_n	CE2_n	R/B1_n		
E			NC	NC	NC	NC	CE3_n	R/B2_n		
F			NC	NC	VREFQ	NC	VSS	R/B3_n		
G			VSP3	VCC	VSP1	NC	NC	VSP2		
H			NC	DQ0	DQS_c	CK_c	CK or WE_0_n	VCCQ		
J			NC	DQ1	DQS	VCCQ	DQ5	DQ7		
K			VSSQ	DQ2	DQ3	DQ4	DQ6	VSSQ		
L	NC	NC							NC	NC
M	NC	NC							NC	NC

Figure 3 — Ball assignments for 8-bit data access, Synchronous DDR data interface

NOTE WE_n is located at ball H7 when a Synchronous DDR capable part is asynchronous SDR mode.

3.1 BGA-63 (Single x8 / x16 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC								NC	NC
C			WP_n	ALE	VSS	CE0_n	WE_n	R/B0_n		
D			VCC	RE_n	CLE	CE1_n	CE2_n	R/B1_n		
E			NC	NC	NC	NC	CE3_n	R/B2_n		
F			NC	NC	NC	NC	VSS	R/B3_n		
G			VSP3	VCC	VSP1	IO13	IO15	VSP2		
H			IO8	IO0	IO10	IO12	IO14	VCCQ		
J			IO9	IO1	IO11	VCCQ	IO5	IO7		
K			VSSQ	IO2	IO3	IO4	IO6	VSSQ		
L	NC	NC							NC	NC
M	NC	NC							NC	NC

Figure 4 — Ball assignments for 16-bit, asynchronous SDR only data access

3.2 BGA-100 (Dual x8 BGA)

Figure 5 defines the ball assignments for devices using NAND Dual x8 BGA packaging with dual 8-bit data access for the asynchronous SDR data interface. Figure 6 defines the ball assignments for devices using NAND Dual x8 BGA packaging with dual 8-bit data access for the Toggle DDR or Synchronous DDR data interface. The minimum package size is 12x18mm and the maximum package size is 14x18mm.

This package uses MO-304.

	1	2	3	4	5	6	7	8	9	10
A	R	R							R	R
B	R									R
C										
D		R	VSP	VSP2_1	WP_1_n	VSP1_1	VSP0_1	VSP	R	
E		R	VSP	VSP2_0	WP_0_n	VSP1_0	VSP0_0	VSP	VDDi	
F		VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	
G		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	
H		VSSQ	VCCQ	R	R	R/B0_1_n	R/B1_1_n or ENo	VCCQ	VSSQ	
J		IO0_1	IO2_1	ALE_1	CE1_1_n	R/B0_0_n	R/B1_0_n	IO5_1	IO7_1	
K		IO0_0	IO2_0	ALE_0	CE1_0_n or ENi	CE0_1_n	CE0_0_n	IO5_0	IO7_0	
L		VCCQ	VSSQ	VCCQ	CLE_1	RE_1_n	VCCQ	VSSQ	VCCQ	
M		IO1_1	IO3_1	VSSQ	CLE_0	RE_0_n	VSSQ	IO4_1	IO6_1	
N		IO1_0	IO3_0	NC	NC	NC	WE_1_n	IO4_0	IO6_0	
P		VSSQ	VCCQ	NC	NC	NC	WE_0_n	VCCQ	VSSQ	
R										
T	R									R
U	R	R							R	R

Figure 5 — Ball assignments for dual 8-bit data access, asynchronous SDR data interface

3.2 BGA-100 (Dual x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10
A	R	R							R	R
B	R									R
C										
D		R	VSP	VSP2_1	WP_1_n	VSP1_1	VSP0_1	VSP	R	
E		R	VSP	VSP2_0	WP_0_n	VSP1_0	VSP0_0	VSP	VDDi	
F		VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	
G		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	
H		VSSQ	VCCQ	VREFQ_1	VREFQ_0	R/B0_1_n	R/B1_0_n or ENo	VCCQ	VSSQ	
J		DQ0_1	DQ2_1	ALE_1	CE1_1_n	R/B0_0_n	R/B1_0_n	DQ5_1	DQ7_1	
K		DQ0_0	DQ2_0	ALE_0	CE1_0_n or ENi	CE0_1_n	CE0_0_n	DQ5_0	DQ7_0	
L		VCCQ	VSSQ	VCCQ	CLE_1	W/R_1_n or RE_1_n	VCCQ	VSSQ	VCCQ	
M		DQ1_1	DQ3_1	VSSQ	CLE_0	W/R_0_n or RE_0_n	VSSQ	DQ4_1	DQ6_1	
N		DQ1_0	DQ3_0	DQS_1_c	DQS_1	RE_1_c	CK_1 or WE_1_n	DQ4_0	DQ6_0	
P		VSSQ	VCCQ	DQS_0_c	DQS_0	RE_0_c	CK_0 or WE_0_n	VCCQ	VSSQ	
R										
T	R									R
U	R	R							R	R

Figure 6 — Ball assignments for dual 8-bit data access, Toggle DDR or Synchronous DDR data interface

3.3 LGA-52

Figure 7 defines the pad assignments for devices using NAND LGA packaging with 8-bit data access. An option is specified for two independent 8-bit data buses. Figure 8 defines the pad assignments for devices using NAND LGA packaging with 16-bit data access. The minimum package size is 12x17mm and the maximum package size is 14x18mm. These NAND LGA packages only support the asynchronous SDR data interface. The indicator (the empty circle in these diagrams) in the lower left of the package is a physical package marker that indicates the appropriate orientation of the package.

The NAND LGA package uses MO-303.

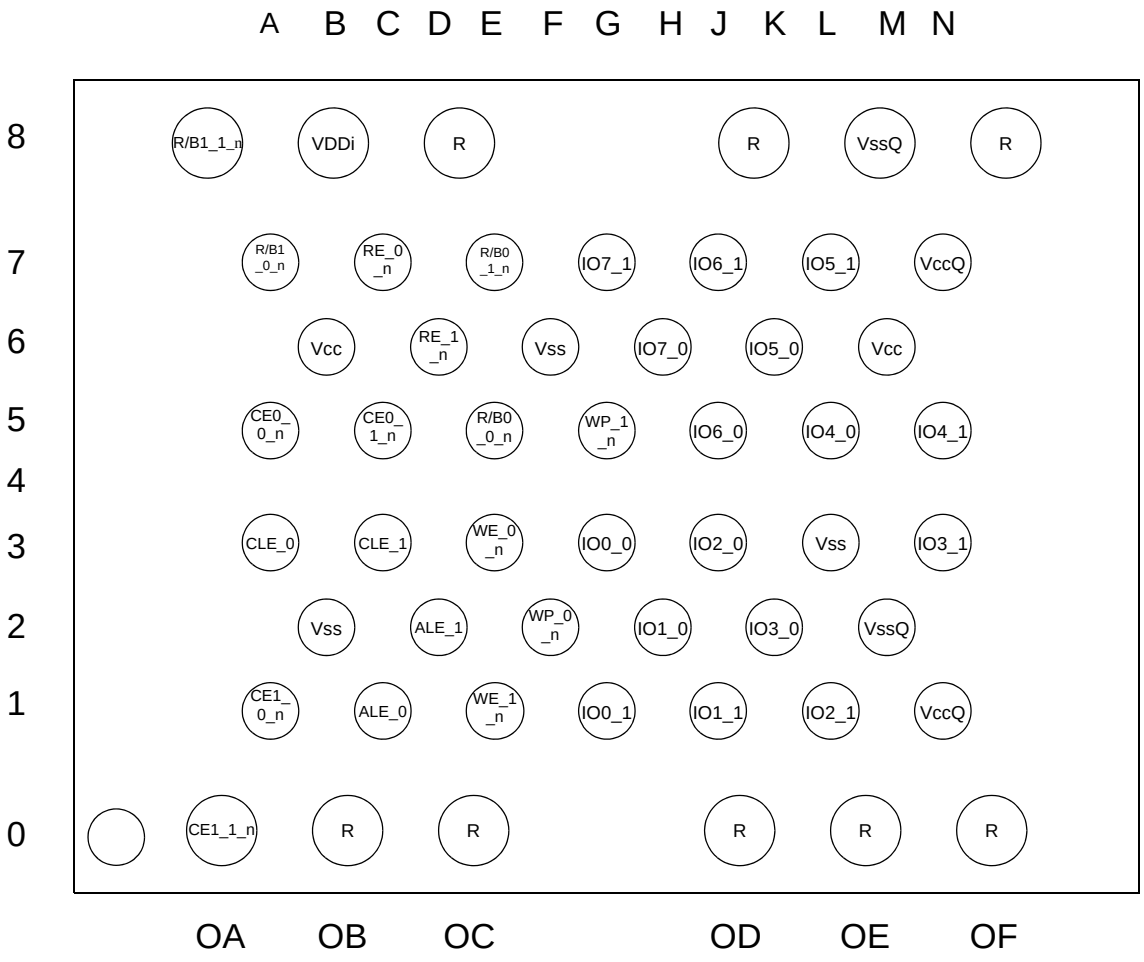

Figure 7 — LGA pinout for 8-bit data access

3.3 LGA-52 (cont'd)

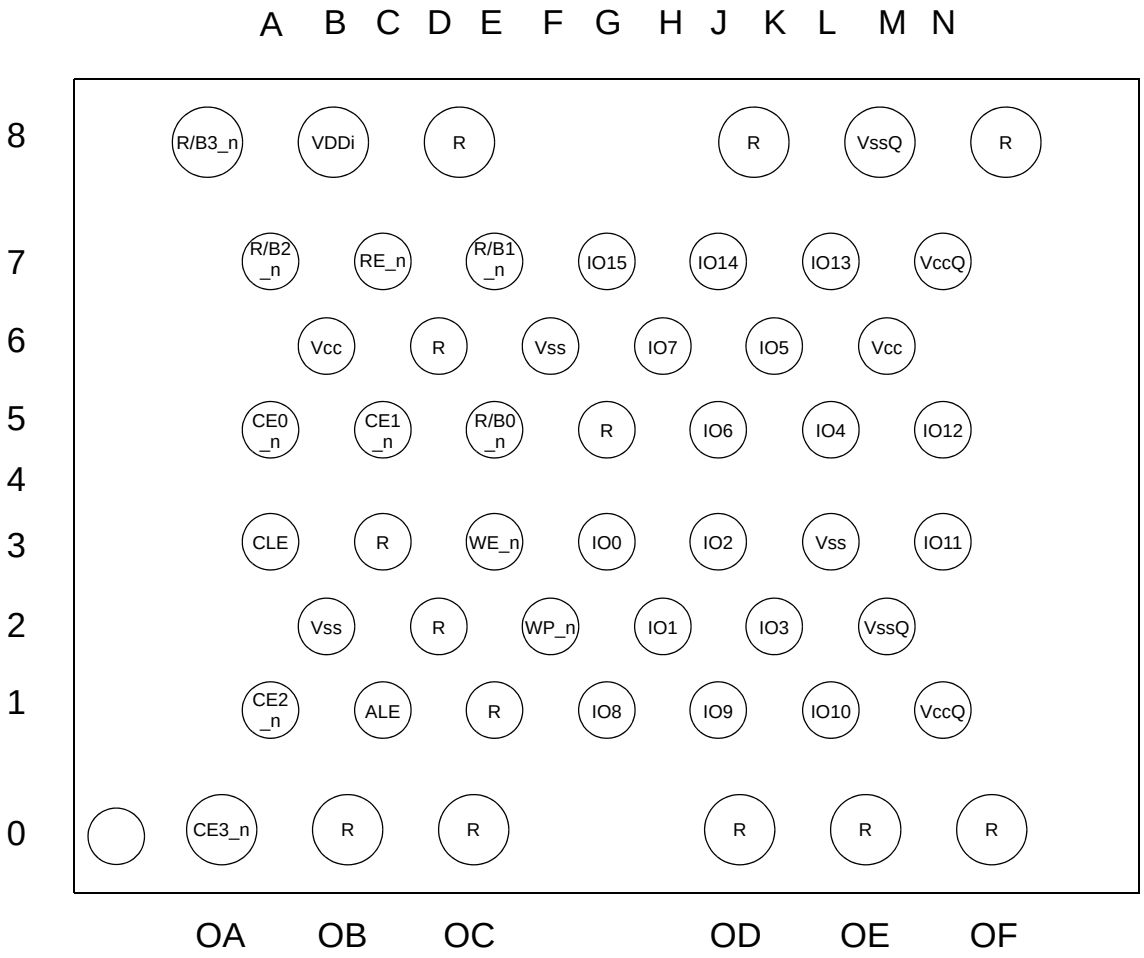

Figure 8 — LGA pinout for 16-bit data access

3.4 BGA-152/132/136 (Dual x8 BGA)

Figure 9 to Figure 11 define the ball assignments for devices using NAND Dual x8 BGA Evolutionary packaging with dual 8-bit data access for the Toggle DDR or Synchronous DDR data interface. Figure 12 to Figure 14 define the ball assignments for devices using NAND Dual x8 BGA Evolutionary packaging with dual 8-bit data access for the asynchronous SDR data interface. 152 BGA is a standard package and 132/136 BGA are the subset packages of 152 BGA for the small size package. NC balls indicate mechanical support balls with no internal connection. NU balls at four corner areas indicate mechanical support balls with possible internal connection. Therefore NU balls landing pad must be isolated. Any of the support ball locations may or may not be populated with a ball depending upon the NAND Flash Vendor's actual package size. Therefore it's recommended to consider landing pad location for all possible support balls based upon maximum package size allowed in the application.

3.4 BGA-152/132/136 (Dual x8 BGA) (cont'd)

The BGA package uses MO-304.

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	NC	NC	NC						NC	NC	NC	NC
B	NC	NC	NC	NC						NC	NC	NC	NC
C	NU	NU	NU	NU						NU	NU	NU	NU
D	NU	NU	VCCQ	VCCQ	DQ3_1	VSS		VCC	DQ4_1	VCCQ	VCCQ	NU	NU
E	NU	NU	VSSQ	DQ2_1	VSSQ	DQS_1 (DQS_1_t)		RE_1_n (RE_1_t) or W/R_1_n	VSSQ	DQ5_1	VSSQ	NU	NU
F			DQ0_1	DQ1_1	DQS_1_c	RE_1_c		WE_1_n or CK_1	VREFQ_1	DQ6_1	DQ7_1		
G			VSSQ	VCCQ	ALE_1	CLE_1		CE3_1_n	CE2_1_n	VCCQ	VSSQ		
H			ENo or NU	ENi or NU	WP_1_n	NU		CE1_1_n	CE0_1_n	NU	NU		
J			VSS	VCC	R/B0_0_n	R/B1_0_n		R/B1_1_n	R/B0_1_n	VCC	VSS		
K			NU	NU	CE0_0_n	CE1_0_n		NU or Vpp	WP_0_n	NU	VDDi or NU		
L			VSSQ	VCCQ	CE2_0_n	CE3_0_n		CLE_0	ALE_0	VCCQ	VSSQ		
M			DQ7_0	DQ6_0	VREFQ_0	WE_0_n or CK_0		RE_0_c	DQS_0_c	DQ1_0	DQ0_0		
N	NU	NU	VSSQ	DQ5_0	VSSQ	RE_0_n (RE_0_t) or W/R_0_n		DQS_0 or (DQS_0_t)	VSSQ	DQ2_0	VSSQ	NU	NU
P	NU	NU	VCCQ	VCCQ	DQ4_0	VCC		VSS	DQ3_0	VCCQ	VCCQ	NU	NU
R	NU	NU	NU	NU						NU	NU	NU	NU
T	NC	NC	NC	NC						NC	NC	NC	NC
U	NC	NC	NC	NC						NC	NC	NC	NC

Figure 9 — NAND Dual x8 BGA-152 package ball assignments for dual 8-bit data access, Toggle DDR or Synchronous DDR data interface

3.4 BGA-152/132/136 (Dual x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	NC						NC	NC	NC
B	NC	NC	NC						NC	NC	NC
C	NU	NU	NU						NU	NU	NU
D	NU	VCCQ	VCCQ	DQ3_1	VSS		VCC	DQ4_1	VCCQ	VCCQ	NU
E	NU	VSSQ	DQ2_1	VSSQ	DQS_1 (DQS_1_t)		RE_1_n (RE_1_t) or W/R_1_n	VSSQ	DQ5_1	VSSQ	NU
F		DQ0_1	DQ1_1	DQS_1_c	RE_1_c		WE_1_n or CK_1	VREFQ_1	DQ6_1	DQ7_1	
G		VSSQ	VCCQ	ALE_1	CLE_1		CE3_1_n	CE2_1_n	VCCQ	VSSQ	
H		ENo or NU	ENi or NU	WP_1_n	NU		CE1_1_n	CE0_1_n	NU	NU	
J		VSS	VCC	R/B0_0_n	R/B1_0_n		R/B1_1_n	R/B0_1_n	VCC	VSS	
K		NU	NU	CE0_0_n	CE1_0_n		NU or Vpp	WP_0_n	NU	VDDi NU	
L		VSSQ	VCCQ	CE2_0_n	CE3_0_n		CLE_0	ALE_0	VCCQ	VSSQ	
M		DQ7_0	DQ6_0	VREFQ_0	WE_0_n or CK_0		RE_0_c	DQS_0_c	DQ1_0	DQ0_0	
N	NU	VSSQ	DQ5_0	VSSQ	RE_0_n (RE_0_t) or W/R_0_n		DQS_0 (DQS_0_t)	VSSQ	DQ2_0	VSSQ	NU
P	NU	VCCQ	VCCQ	DQ4_0	VCC		VSS	DQ3_0	VCCQ	VCCQ	NU
R	NU	NU	NU						NU	NU	NU
T	NC	NC	NC						NC	NC	NC
U	NC	NC	NC						NC	NC	NC

Figure 10 — NAND Dual x8 BGA-132 package ball assignments for dual 8-bit data access, Toggle DDR or Synchronous DDR data interface

3.4 BGA-152/132/136 (Dual x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	NC	NC	NC						NC	NC	NC	NC
B	NU	NU	NU	NU						NU	NU	NU	NU
C	NU	NU	VCCQ	VCCQ	DQ3_1	VSS		VCC	DQ4_1	VCCQ	VCCQ	NU	NU
D	NU	NU	VSSQ	DQ2_1	VSSQ	DQS_1 (DQS_1_t)		RE_1_n (RE_1_t) or W/R_1_n	VSSQ	DQ5_1	VSSQ	NU	NU
E			DQ0_1	DQ1_1	DQS_1_c	RE_1_c		WE_1_n or CK_1	VREFQ_ 1	DQ6_1	DQ7_1		
F			VSSQ	VCCQ	ALE_1	CLE_1		CE3_1_n	CE2_1_n	VCCQ	VSSQ		
G			ENo or NU	ENi or NU	WP_1_n	NU		CE1_1_n	CE0_1_n	NU	NU		
H			VSS	VCC	R/B0_0_n	R/B1_0_n		R/B1_1_n	R/ B0_1_n	VCC	VSS		
J			NU	NU	CE0_0_n	CE1_0_n		NU or Vpp	WP_0_n	NU	VDDi or NU		
K			VSSQ	VCCQ	CE2_0_n	CE3_0_n		CLE_0	ALE_0	VCCQ	VSSQ		
L			DQ7_0	DQ6_0	VREFQ_ 0	WE_0_n or CK_0		RE_0_c	DQS_0_c	DQ1_0	DQ0_0		
M	NU	NU	VSSQ	DQ5_0	VSSQ	RE_0_n (RE_0_t) or W/R_0_n		DQS_0 (DQS_0_t)	VSSQ	DQ2_0	VSSQ	NU	NU
N	NU	NU	VCCQ	VCCQ	DQ4_0	VCC		VSS	DQ3_0	VCCQ	VCCQ	NU	NU
P	NU	NU	NU	NU						NU	NU	NU	NU
R	NC	NC	NC	NC						NC	NC	NC	NC

Figure 11 — NAND Dual x8 BGA-136 package ball assignments for dual 8-bit data access, Toggle DDR or Synchronous DDR data interface

3.4 BGA-152/132/136 (Dual x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	NC	NC	NC						NC	NC	NC	NC
B	NC	NC	NC	NC						NC	NC	NC	NC
C	NU	NU	NU	NU						NU	NU	NU	NU
D	NU	NU	VCCQ	VCCQ	DQ3_1	VSS		VCC	DQ4_1	VCCQ	VCCQ	NU	NU
E	NU	NU	VSSQ	DQ2_1	VSSQ	NU		RE_1_n	VSSQ	DQ5_1	VSSQ	NU	NU
F			DQ0_1	DQ1_1	NU	NU		WE_1_n	NU	DQ6_1	DQ7_1		
G			VSSQ	VCCQ	ALE_1	CLE_1		CE3_1_n	CE2_1_n	VCCQ	VSSQ		
H			ENo or NU	ENi or NU	WP_1_n	NU		CE1_1_n	CE0_1_n	NU	NU		
J			VSS	VCC	R/B0_0_n	R/B1_0_n		R/B1_1_n	R/B0_1_n	VCC	VSS		
K			NU	NU	CE0_0_n	CE1_0_n		NU or Vpp	WP_0_n	NU	VDDi or NU		
L			VSSQ	VCCQ	CE2_0_n	CE3_0_n		CLE_0	ALE_0	VCCQ	VSSQ		
M			DQ7_0	DQ6_0	NU	WE_0_n		NU	NU	DQ1_0	DQ0_0		
N	NU	NU	VSSQ	DQ5_0	VSSQ	RE_0_n		NU	VSSQ	DQ2_0	VSSQ	NU	NU
P	NU	NU	VCCQ	VCCQ	DQ4_0	VCC		VSS	DQ3_0	VCCQ	VCCQ	NU	NU
R	NU	NU	NU	NU						NU	NU	NU	NU
T	NC	NC	NC	NC						NC	NC	NC	NC
U	NC	NC	NC	NC						NC	NC	NC	NC

Figure 12 — NAND Dual x8 BGA-152 package ball assignments for dual 8-bit data access, asynchronous SDR data interface

3.4 BGA-152/132/136 (Dual x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	NC						NC	NC	NC
B	NC	NC	NC						NC	NC	NC
C	NU	NU	NU						NU	NU	NU
D	NU	VCCQ	VCCQ	DQ3_1	VSS		VCC	DQ4_1	VCCQ	VCCQ	NU
E	NU	VSSQ	DQ2_1	VSSQ	NU		RE_1_n	VSSQ	DQ5_1	VSSQ	NU
F		DQ0_1	DQ1_1	NU	NU		WE_1_n	NU	DQ6_1	DQ7_1	
G		VSSQ	VCCQ	ALE_1	CLE_1		CE3_1_n	CE2_1_n	VCCQ	VSSQ	
H		ENo or NU	ENi or NU	WP_1_n	NU		CE1_1_n	CE0_1_n	NU	NU	
J		VSS	VCC	R/B0_0_n	R/B1_0_n		R/B1_1_n	R/B0_1_n	VCC	VSS	
K		NU	NU	CE0_0_n	CE1_0_n		NU or Vpp	WP_0_n	NU	VDDi or NU	
L		VSSQ	VCCQ	CE2_0_n	CE3_0_n		CLE_0	ALE_0	VCCQ	VSSQ	
M		DQ7_0	DQ6_0	NU	WE_0_n		NU	NU	DQ1_0	DQ0_0	
N	NU	VSSQ	DQ5_0	VSSQ	RE_0_n		NU	VSSQ	DQ2_0	VSSQ	NU
P	NU	VCCQ	VCCQ	DQ4_0	VCC		VSS	DQ3_0	VCCQ	VCCQ	NU
R	NU	NU	NU						NU	NU	NU
T	NC	NC	NC						NC	NC	NC
U	NC	NC	NC						NC	NC	NC

Figure 13 — NAND Dual x8 BGA-132 package ball assignments for dual 8-bit data access, asynchronous SDR data interface

3.4 BGA-152/132/136 (Dual x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	NC	NC	NC						NC	NC	NC	NC
B	NU	NU	NU	NU						NU	NU	NU	NU
C	NU	NU	VCCQ	VCCQ	DQ3_1	VSS		VCC	DQ4_1	VCCQ	VCCQ	NU	NU
D	NU	NU	VSSQ	DQ2_1	VSSQ	NU		RE_1_n	VSSQ	DQ5_1	VSSQ	NU	NU
E			DQ0_1	DQ1_1	NU	NU		WE_1_n	NU	DQ6_1	DQ7_1		
F			VSSQ	VCCQ	ALE_1	CLE_1		CE3_1_n	CE2_1_n	VCCQ	VSSQ		
G			ENo or NU	ENi or NU	WP_1_n	NU		CE1_1_n	CE0_1_n	NU	NU		
H			VSS	VCC	R/B0_0_n	R/B1_0_n		R/B1_1_n	R/B0_1_n	VCC	VSS		
J			NU	NU	CE0_0_n	CE1_0_n		NU or Vpp	WP_0_n	NU	VDDi or NU		
K			VSSQ	VCCQ	CE2_0_n	CE3_0_n		CLE_0	ALE_0	VCCQ	VSSQ		
L			DQ7_0	DQ6_0	NU	WE_0_n		NU	NU	DQ1_0	DQ0_0		
M	NU	NU	VSSQ	DQ5_0	VSSQ	RE_0_n		NU	VSSQ	DQ2_0	VSSQ	NU	NU
N	NU	NU	VCCQ	VCCQ	DQ4_0	VCC		VSS	DQ3_0	VCCQ	VCCQ	NU	NU
P	NU	NU	NU	NU						NU	NU	NU	NU
R	NC	NC	NC	NC						NC	NC	NC	NC

Figure 14 — NAND Dual x8 BGA-136 package ball assignments for dual 8-bit data access, asynchronous SDR data interface

4 Command Sets for NAND Flash memory

4.1 Basic Command Definition

Table 2 outlines the commands defined for NAND Flash memory.

The value specified in the first command cycle identifies the command to be performed. Some commands have a second command cycle as specified in Table 2. Typically, commands that have a second command cycle include an address.

Table 2 — Command set

Command	O/M	1st Cycle	2nd Cycle	Acceptable while Accessed LUN is Busy	Acceptable while Other LUNs are Busy	Target level commands
Page Read	M	00h	30h		Y	
Copyback Read	O	00h	35h		Y	
Change Read Column	M	05h	E0h		Y	
Read Cache Random	O	00h	31h		Y	
Read Cache Sequential	O	31h	na		Y	
Read Cache End	O	3Fh	na		Y	
Block Erase	M	60h	D0h		Y	
Page Program	M	80h	10h		Y	
Copyback Program	O	85h	10h		Y	
Change Write Column	M	85h	na		Y	
Get Features	O	EEh	na			Y
Set Features	O	EFh	na			Y
Page Cache Program	O	80h	15h		Y	
Read Status	M	70h	na	Y		
Read Unique ID	O	EDh	na			Y
Reset	M	FFh	na	Y	Y	Y
Synchronous Reset	O	FCh	na	Y	Y	Y
Reset LUN	O	FAh		Y	Y	

4.2 Primary & Secondary Command Definition For the Advanced Operation

Table 3 defines the Primary and Secondary Commands. Primary commands are the recommended implementation for a particular command. Secondary commands are an alternate implementation approach that is allowed for backwards compatibility. All commands are optional. Commands may be used with any data interface (asynchronous SDR, Toggle DDR, or Synchronous DDR).

Table 3 — Primary and Secondary Commands

Command	O/M	Primary or Secondary	1st Cycle	2nd Cycle	ONFI or Toggle-mode Heritage (remove in future)
Multi-plane Read	O	Primary	00h	32h	ONFI
		Secondary	60h	30h	Toggle-mode
Multi-plane Read Cache Random	O	Primary	00h	31h	ONFI
		Secondary	60h	3Ch	Toggle-mode
Multi-plane Copyback Read	O	Primary	00h	35h	ONFI
		Secondary	60h	35h	Toggle-mode
Random Data Out	O	Primary	00h 05h	n/a E0h	Toggle-mode
		Secondary	06h	E0h	ONFI
Multi-plane Program	O	Primary	80h or 81h	11h	Toggle-mode
		Secondary	80h	11h	ONFI
Multi-plane Copyback Program	O	Primary	85h or 81h	11h	Toggle-mode
		Secondary	85h	11h	ONFI
Multi-plane Block Erase	O	Primary	60h	n/a	Toggle-mode
		Secondary	60h	D1h	ONFI
Read Status Enhanced	O	Primary	78h	n/a	ONFI
		Secondary	F1h/F2h	n/a	Toggle-mode

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