Simplifying Flash Controller Design

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Abstract

Unlike the DRAM (Dynamic RAM), which is an industry standard multi-sourced component, suppliers of NAND Flash have introduced products with proprietary features and “similar” electrical specifications. This complicates system design; since the host controller design has to undergo a major hardware and firmware overhaul to accommodate a new component, delaying product development while increasing costs. The Open NAND Flash Interface (ONFi) organization comprises suppliers and developers of NAND Flash memory components whose goal is to define a uniform NAND Flash component interface. The uniform interface provides the means for an application to seamlessly use a wide range of disparate NAND Flash.

This white paper highlights ONFi’s efforts to alleviate system design problems caused by the lack of standardization of NAND Flash. This standardization is necessary to support the continued proliferation of NAND Flash into new applications such as PMP (Personal Media Players) and solid state disks, as well as migration into the PC platform as cache to enable fast boot.

The Curse of “Similarity”

Although all currently available NAND Flash components exhibit similar behavior, they have subtle differences that must be recognized by the host controller. To do this the host maintains a chip ID table of all supported devices incorporating all the differences. This ID table is programmed into the host controller’s ROM (Read Only Memory) and any changes would require an overhaul of controller firmware – an expensive and time consuming effort. This means any new component introduced by a supplier cannot be designed in the system.

Variations in these “similar” NAND Flash components are numerous and include Basic Commands, Timing, Status Values and Read ID differences.

Basic Commands:

Command sets between suppliers vary considerably due to the numerous proprietary features of the device. Table 1 below illustrates the differences between the command sets of two industry leading suppliers. Some of the Commands between the two suppliers are identical. Vendor ‘B’ offers seven additional commands not offered by Vendor ‘A’. The common commands are highlighted in color.

Function	1st Cycle	2nd Cycle
Read	**00h**	**30h**
Read for Copy Back	**00h**	**35h**
Read ID	**90h**	**-**
Reset	**FFh**	**-**
Page Program	**80h**	**10h**
Cache Program	**80h**	**15h**
Copy-Back Program	**85h**	**10h**
Block Erase	**60h**	**D0h**
Random Data Input	**85h**	**-**
Random Data Output	**05h**	**E0h**
Read Status	**70h**	**-**

Vendor ‘A’ Basic Commands

Function	1st Cycle	2nd Cycle
Read 1	**00h**	**30h**
Read for Copy Back	**00h**	**35h**
Read ID	**90h**	**-**
Reset	**FFh**	**-**
Page Program(start)	**80h**	**10h**
Cache-Back Program(start)	**85h**	**10h**
Cache Program	**80h**	**15h**
Block Erase	**60h**	**D0h**
Read Status Register	**70h**	**-**
Random Data Input	**85h**	**-**
Random Data Output	**05h**	**E0h**
Cache Read (start)	00h	31h
Cache Read(exit)	34h	
Lock Block	2Ah	
Lock Tight	2Ch	
Unlock(start area)	23h	
Unlock(end area)	24h	
Read Lock Status	7Ah	

Vendor ‘B’ Basic Commands

Table 1. Variations in Basic Commands

Other NAND Flash Variations

Differences exist in device timing parameters as well with, wide variations in minimum/maximum values and test conditions of these parameters. Status values that identify the operational status of a device for like Commands are not always identical for all suppliers'. However, vendors are free to assign any status values to their specific products. Likewise, Read ID table, that allows the host to identify a certain Flash component, is vendor specific. Table 2 below illustrates these differences. The status values that are common between the two suppliers are highlighted in color.

Byte	Description
1st	**Maker Code**
2nd	**Device Code**
3rd	Don't Care
4th	Page Size, Block Size, Spare Size, Organization

Vendor 'A' Read ID

Data	Description
1st	**Maker Code**
2nd	**Device Code**
3rd	Chip No., Cell Type, PGM Page, Write Cache

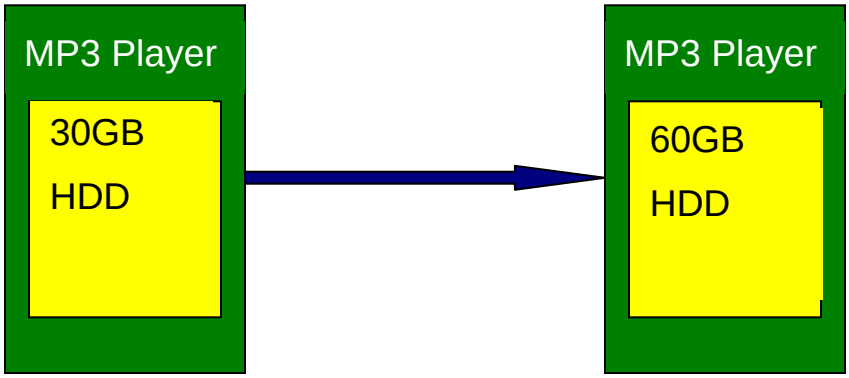
Vendor 'B' read ID

Table 2. Read ID Variations between Suppliers

The complexity of accommodating these variations in device specifications multiplies with the wide range of products, densities, technologies, process geometries and suppliers delivering 'similar' but not fully compatible products. Not only must the host controller hardware be designed to accommodate the range of behaviors, but the controller firmware must have a list (Chip ID Table) of all these variations by supplier, density, technology, features, etc, so as to allow use of the Flash component in an application. These are hard-wired in the Read Only Memory (ROM) resident in the controller. Any new component cannot be used in the same application without modifications to the controller hardware and firmware.

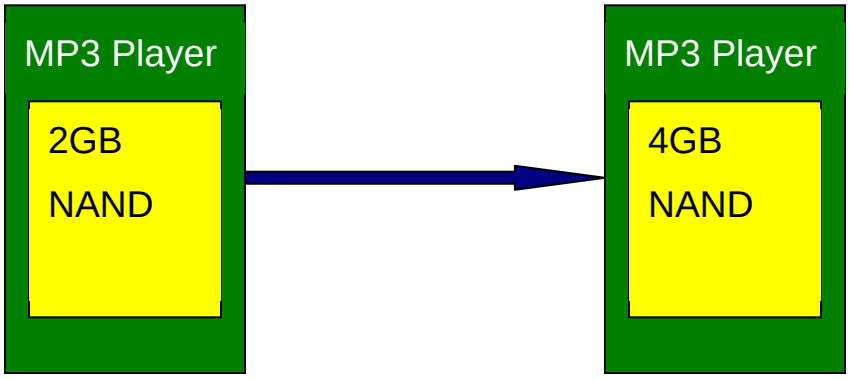
Memory vendors are generally inclined to add features to products to meet a customer's specific system design needs with the hope of gaining a competitive advantage and commanding price premiums. This usually invariably results in minimal market opportunities, a situation similar to the competing standards for video recording, BetaMax and VHS of the past, and Blu-Ray and HD-DVD optical disk formats of the present.

As a result of declining price-per-bit, applications such as MP3 players have replaced hard disk drives (HDDs) in favor of NAND Flash which offer superior mechanical ruggedness and performance advantages. However, compared to HDDs, upgrading a current MP3 design with new NAND Flash components can be a major challenge. Such an upgrade with NAND Flash components would require firmware or software changes in the host controller with changes in the ID Table followed by an extensive test and qualification to ensure stability of the new design. An upgrade to a HDD based platform is much simpler since the components are standardized and have the same specifications. The pictorial below, Figure 1(a) and 1(b), illustrates the problem



- No software changes required
- Product level testing and qualifying

Figure 1(a). Design Upgrade Simple with HDD



- Firmware and software changes required
  - Changes in ID Table to support new component
  - Add support for new commands
- Complete retest of firmware and software

Figure 1(b). Design Upgrade complexities with NAND

Lack of standards adversely impacts the adoption of NAND Flash components despite their putative similarities as illustrated above.

ONFi Standardization :

As of December 28th, 2006, ONFi has released revision 1.0 of the Open NAND Flash Interface that standardizes on the device behaviors including those discussed earlier in this document. Besides defining a uniform set of Commands, Timing parameters and pin-outs for x8 and x16 component organizations, the specification provides self-describe features via a Read Parameter Table. This table 'identifies' the Flash component vis-a-vis its design organization, features, timings, and other behavioral parameters in order to eliminate the need for a controller to carry such information in its ROM microcode. This table, a section of which is shown in Figure 2, is standard for all suppliers adhering to the ONFi specification, thus simplifying the host controller design and facilitating the adoption of NAND Flash components offered by multiple sources.

Number of Data Bytes per Page
Number of Redundant Bytes per Page
Number of Pages per Block
Number of Blocks per Logical Unit
Number of Logical Units
Number of Address Cycles
Number of bits per cell
Block endurance
Number of programs per Page
Recommended bits for ECC
Interleaved Addressing

Figure 2. A section of the Parameter Read Page

The ONFi specification, however, does permit NAND Flash suppliers to offer unique parametric or functional advantages to their products.

Future ONFi Developments

Standardization of the existing NAND Flash protocol was the first phase of ONFi. The NAND Flash memory has enormous opportunities for significant performance and functionality improvements, which may be harvested with a unified standardization effort.

Timing Enhancements

Unlike modern double data rate (DDR) DRAM, NAND Flash is not source synchronous. A source-synchronous device uses a strobe or a clock signal to accurately latch the signal at the output, enabling higher frequencies to be realized. Providing a strobe at the output eliminates the flight time variable in system design maximizing the

bandwidth. ONFi is pursuing various approaches to improve timing parameters and increase transfer rates. These include specifying a source sycnhronous interface (a la DDR DRAM) on future NAND Flash memory to support higher frequencies and further increasing transfer rates with DDR signalling.

To improve performance through increased concurrency, ONFi is adding features such as Interleaved operations. Interleaving may be used to complete the same operation on additional blocks of data to enhance performance. This technique is quite commonly used in memory subsystem design. The two methods under consideration are (1) Concurrent Interleaving, where operations to multiple blocks is issued at the same time and then executed in parallel, and (2) Overlapped Interleaving, where the operations are issued independently allowing the host controller to determine the sequence of execution. Interleaved operations include reads, programs and erases.

Block Abstraction

Current NAND Flash devices feature physical–address access that defines each physical memory array to the block, to the page down to the byte of data. The driver in the host controller must recognize and accomodate this complicated physical addressing. Any change in device density requires modifications to the driver in the host controller, hindering use of the new component.

Block abstraction simplifies host controller design by allowing the host to treat the Flash as a pool of addressable blocks of data, without having to manage those blocks. Block Abstraction (BA), therefore, eliminates the sensitivity host controllers might have to changes in NAND Flash device requirements such as advanced ECC, that cannot be readily accomodated without host controller redesign.

BA frees the host controller from the traditional NAND-specific functions such as ECC (Error Correction and Checking), wear-leveling, and bad block management, which may now be performed by the NAND Flash controller along with other Flash memory management functions. The emergence of MLC (Multi-Level Cell) NAND requires the use of advanced ECC and complex software drivers. BA would simplify the overall system design.

This method of addressing the memory is similar to what is used currently in hard drives, whereby the drive is accessed by linearly addressing sector addresses. Figures 3 and Figure 4 show the differences in the two NAND Flash architectures.

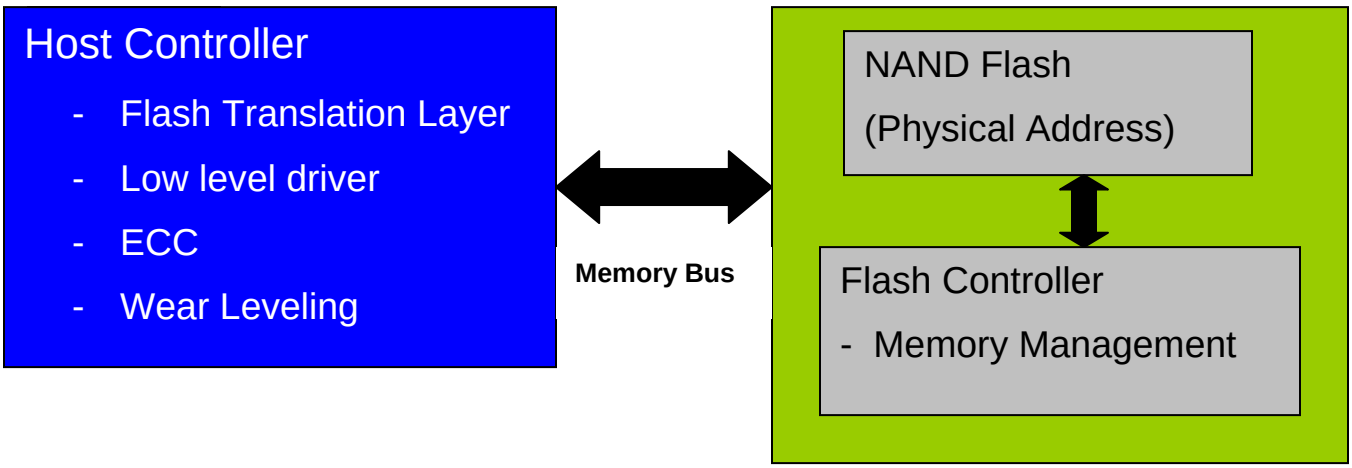


Figure 3. Diagram of Physical Addressed NAND based System

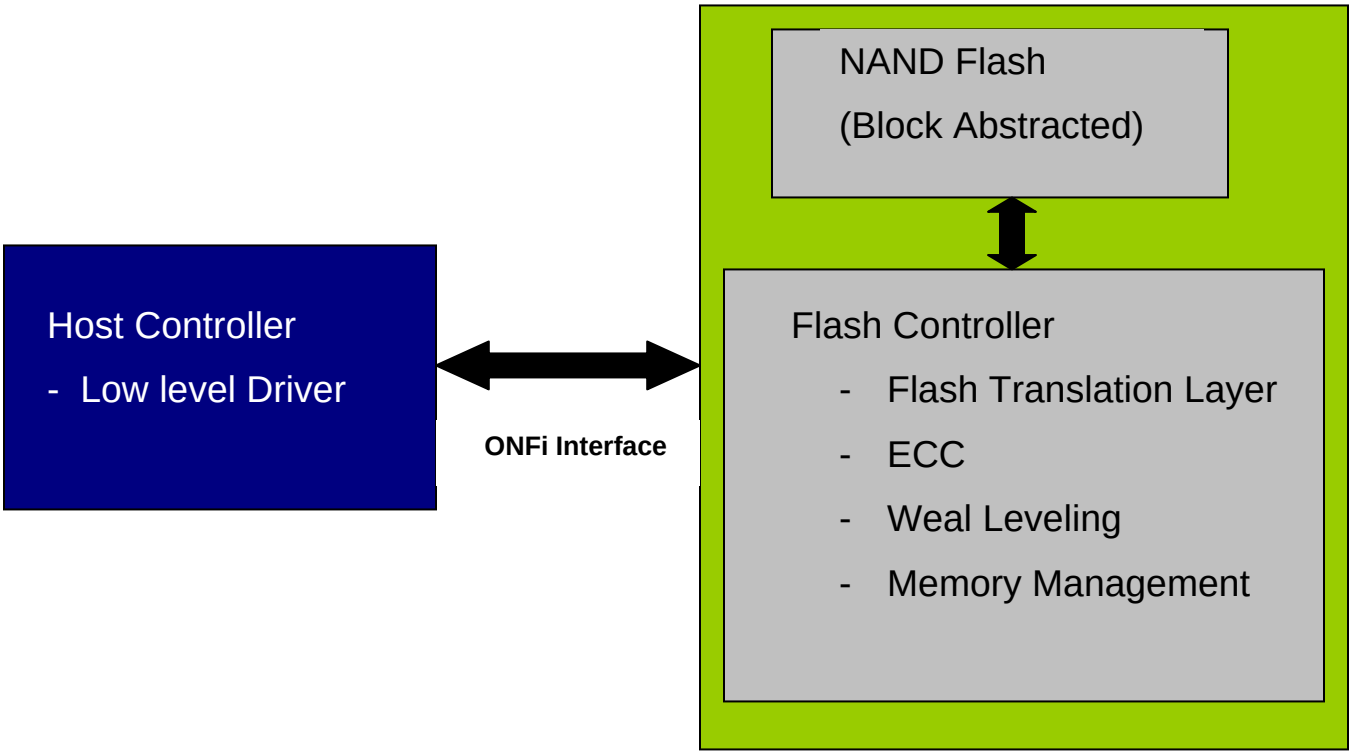


Figure 4. Diagram of Block Abstracted NAND based System

NAND Connection

There is currently no DRAM DIMM-like solution for NAND Flash, which would allow Flash to be connected to a platform via an industry standard connector. Using a NAND Flash DIMM, a PC/Notebook could be easily enhanced with Flash to provide benefits such as faster boot, improved applications responsiveness, and reduced power consumption. The faster read/write feature on the NAND Flash enables both read and write caching to the hard disk drive. This allows the non-volatile cache unit to

supply data to the system CPU much faster than from magnetic storage. The booting process and speed is substantially improved with boot files stored in NAND Flash cache while reducing power consumption as a result of reduction in accesses to the disk (Table 3).

Feature	HDD	NAND Flash Cache
Access Latency(ms)	~7.5	~0.06
Boot Time (Seconds)	--	~30 seconds faster
Battery Life (Min)	--	~30 minutes longer

Table 3. NAND Flash Cached Application

Summary

ONFi's efforts, which began with standardizing NAND Flash component pin-outs, timing and features, is now moving into the next phase. The new phase involves improving speed and functionality by adding elements such as higher transfer rates, interleaving, block abstraction, and a module connector solution to the NAND Flash – all aligned to a standard specification.

This effort should help NAND Flash suppliers since the standardization facilitates the design of new components into current or future applications. Users of NAND Flash also benefit from the simplification of system upgrades and integration of Flash components into new designs.

Industry standard component pin-out and packaging ensures easy system upgrade without the need for redesign of the PCB.